



# KBY3-LT Rev:1.0

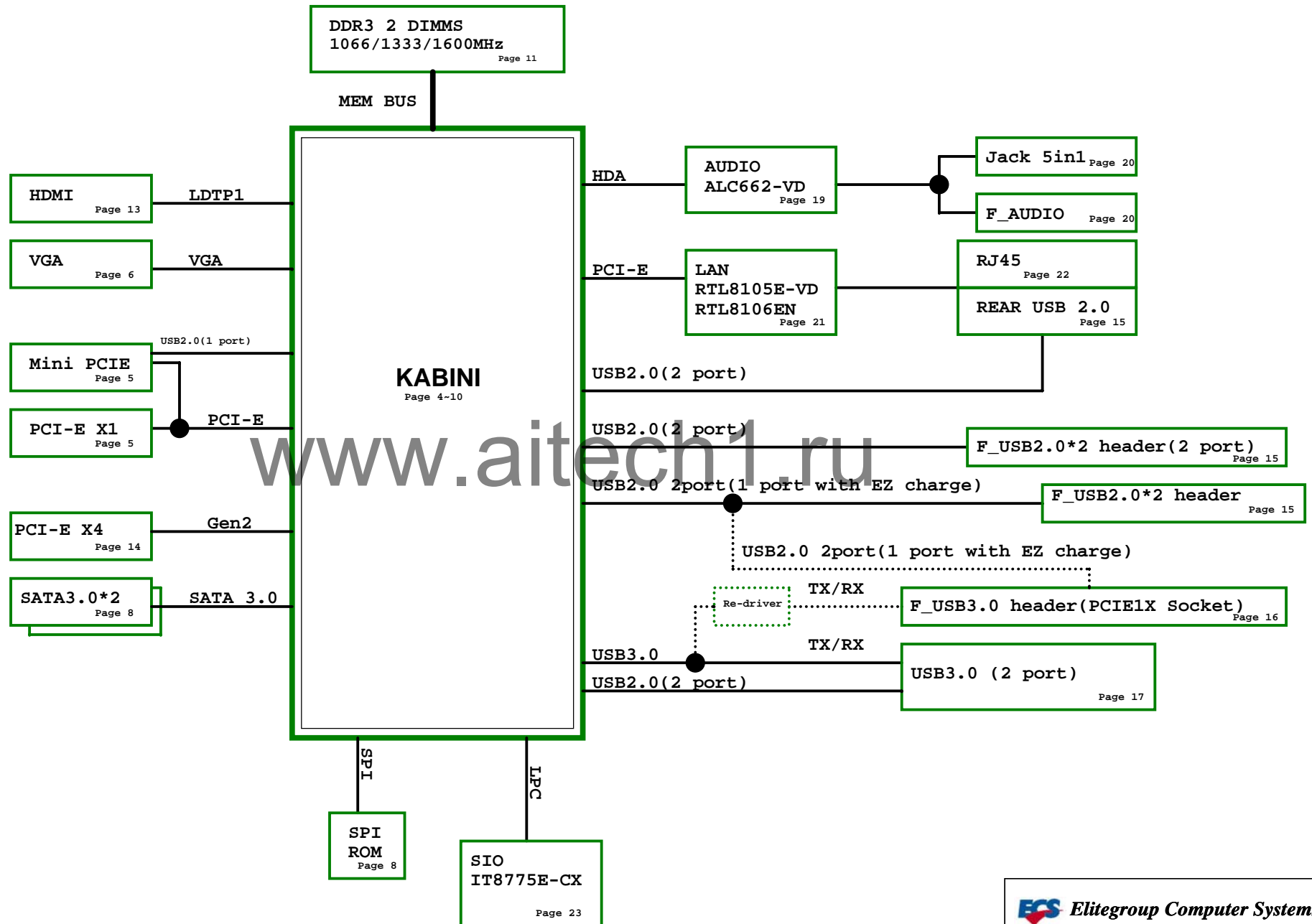
ECS  
CONFIDENTIAL

IPG:H515

AMD KABINI Platform

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APU-GPIO Function

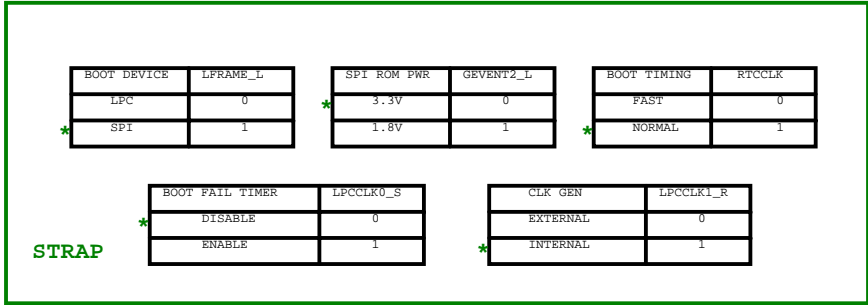
Interrupt mapping


Pin Name	Power Well	Usage	Default Status	Boot Set	Function	INT# port	PCle*1 port	Device
GPIO56	VCC3	RESERVE GPIO	FANIN0	GPI	PCIE1X1	INTC#	Port 1	PCIE 1X
GPIO55	VCC3	Front Audio detect		GPI	LAN	INTB#	Port 2	RTL8105E
GPIO59	VCC3	CASE GPIO	GPIO	GPI	MINI PCIE	INTD#	Port 3	MINI PCIE
GPIO61	VCC3	GFX DETECT	CLK_REQ1_L	GPI	PCIE16X1	INTB#	PCIE X4	
GPIO64	VCC3	CASE GPIO	GPIO	GPI	SATA	INTB#		
GPIO68	VCC3	RESERVE GPIO	GPIO	GPI				
GPIO69	VCC3	RESERVE GPIO	GPIO	GPI				
GPIO70	VCC3	RESERVE GPIO	GPIO	GPI				
GPIO71	VCC3	RESERVE GPIO	GPIO	GPI				
GPIO174	3VSB	CLEAR CMOS	GPIO	GPI				
GPIO168	1.5VSB	USB CHARGE	AZ_SDIN1	GPO				
GPIO169	1.5VSB	USB CHARGE	AZ_SDIN2	GPO				
GPIO170	1.5VSB	USB CHARGE	AZ_SDIN3	GPO				
GPIO184	3VSB	WLAN DISABLE	IR LED	GPO				

SIO-GPIO Function

Pin Name	Power Well	Usage	Default Status	Boot Set
GPIO23	3VSB	FP LED0	CPU_PG	GPO
GPIO41	3VSB	FP LED1	SIN1	GPO
GPIO31	VCC3	BEEP	CST1#	GPO
GPIO10	3VSB	THERMAL ALERT	PCIRST3#	GPI
GPIO45	3VSB	Charge Enable	DSR1	GPO
GPIO65	3VSB	RESERVE GPIO	VLDT_EN	GPI

2012-02-23 V0.3  
Reserved USBCHA\_EN to SIO GP45





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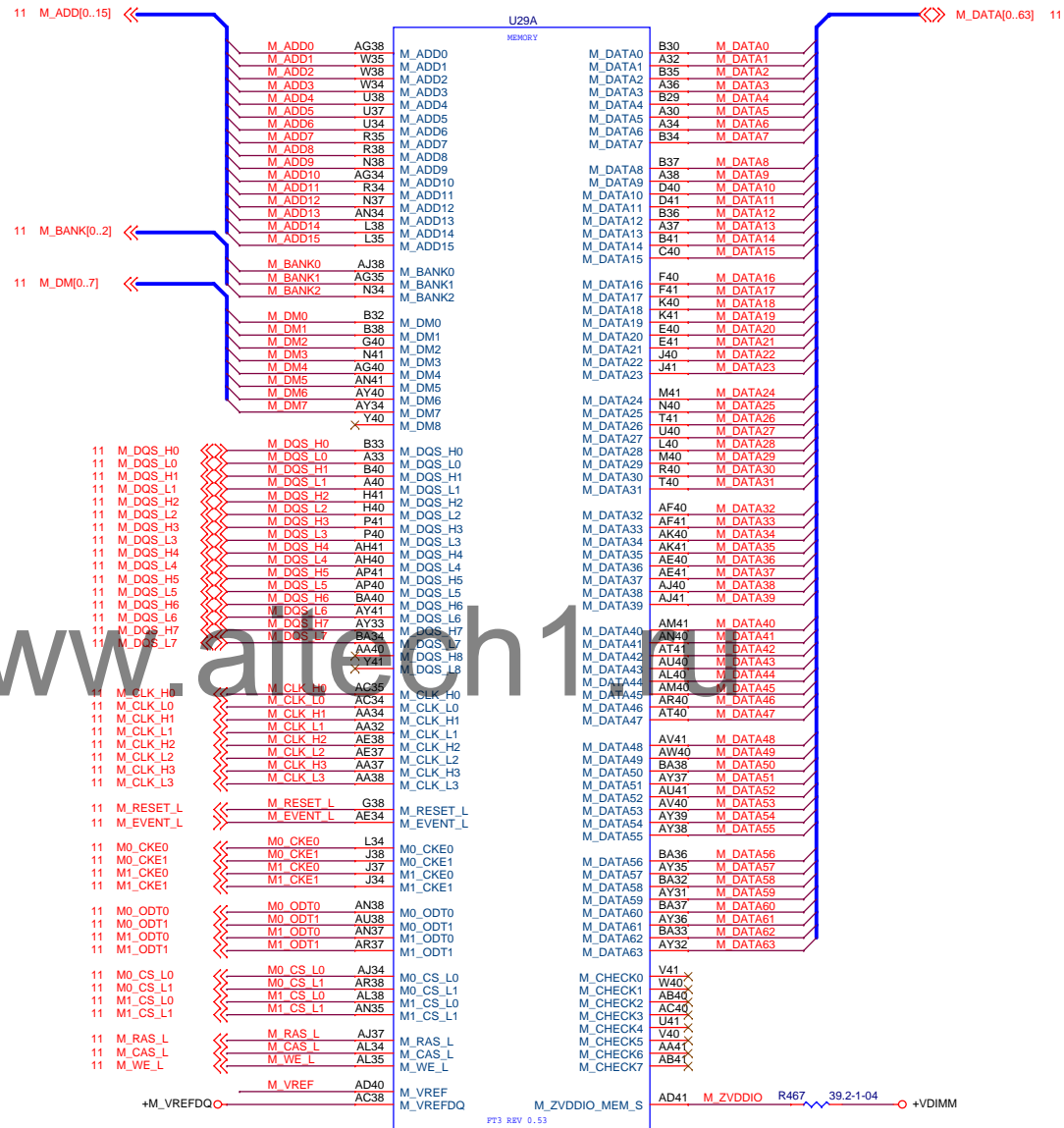
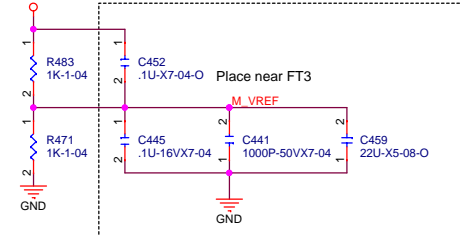
Title: **INIT# & GPIO Function**

Size: Custom    Document Number: **KBY3-LT**    Rev: **1.0**

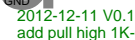
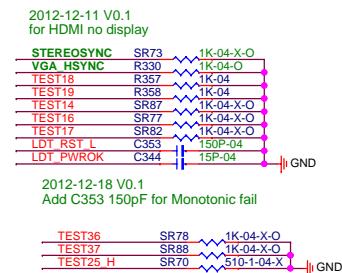
Date: **Friday, April 19, 2013**    Sheet: **3** of **36**

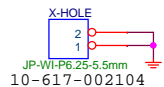
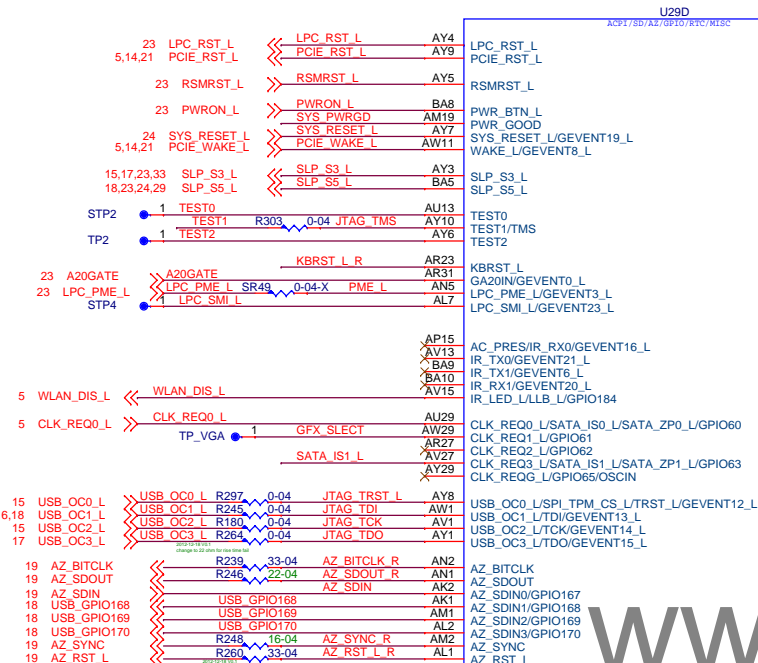
+VDIMM SR95 1 2 1K-04-X M\_EVENT\_L

+VDIMM

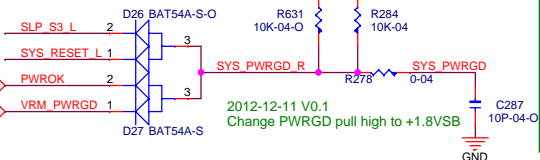








2012-12-11 V0.1  
Change to 18pF for SI



2012-12-11 V0.1  
Change PWRGD pull high to +1.8VSB

#### Strap PIN

BOOT DEVICE	LFRAME_L
LPC	0
SPI	1

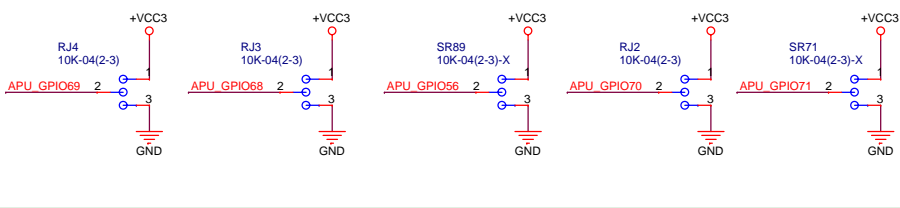
#### Strap PIN

SPI ROM PWR	GEVENT2_L
3.3V	0
1.8V	1

#### Strap PIN

BOOT TIMING	RTCCCLK
FAST	0
NORMAL	1

#### Reserve GPIOs



GPIO SELECT	GPIO_SELECT
INTERNAL	1
EXTERNAL	0

\*

#### Strap PIN

BOOT FAIL TIMER	LPCCCLK0_S
DISABLE	0
ENABLE	1

#### Strap PIN

CLK GEN	LPCCCLK1_R
EXTERNAL	0
INTERNAL	1

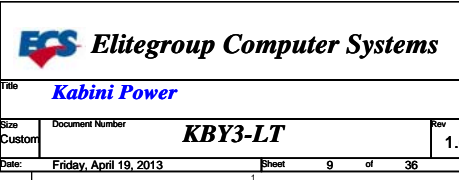
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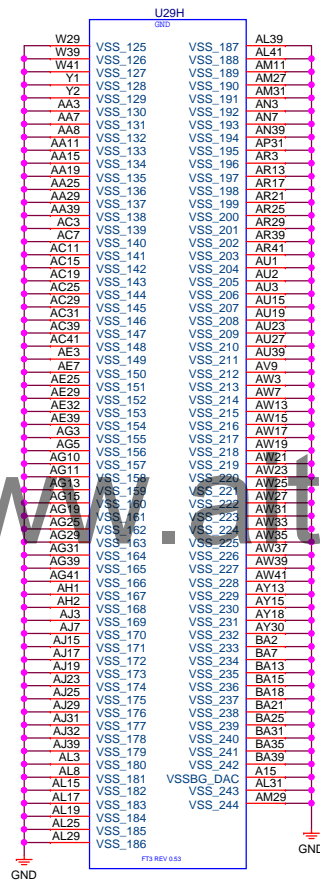
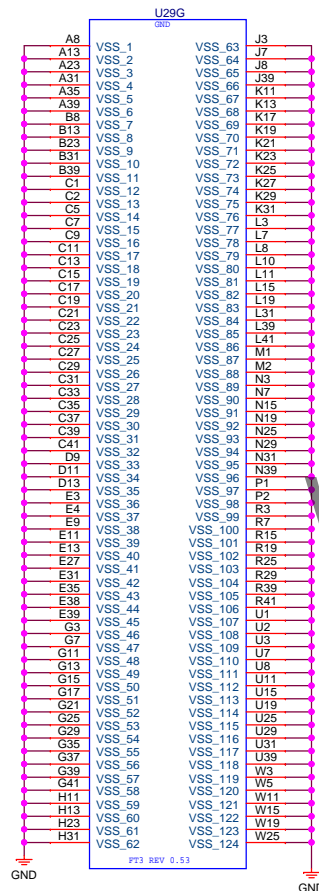
Kabini MISC\_SD\_GPIO\_STRAP



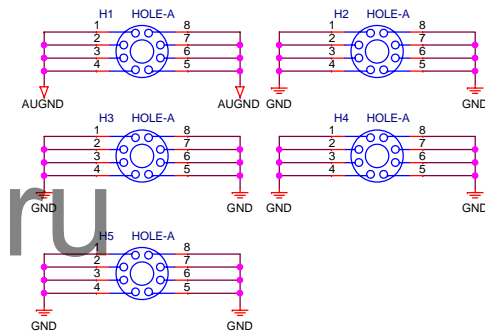
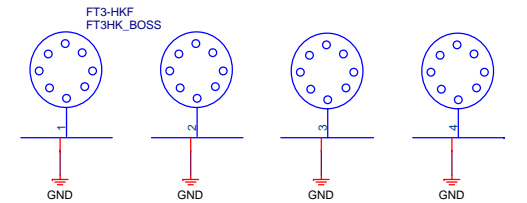




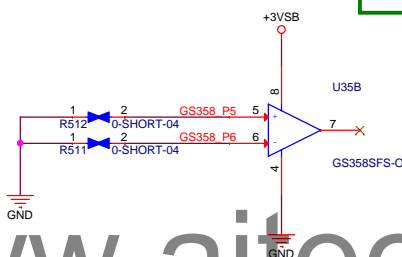
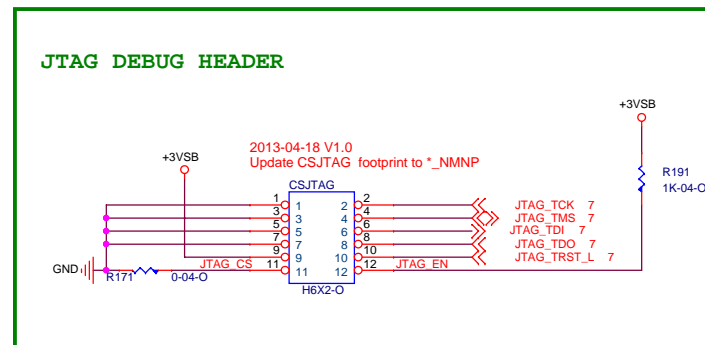
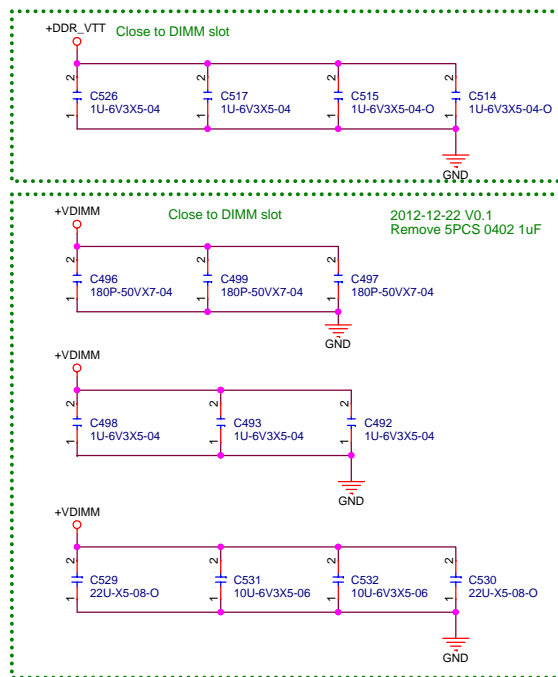




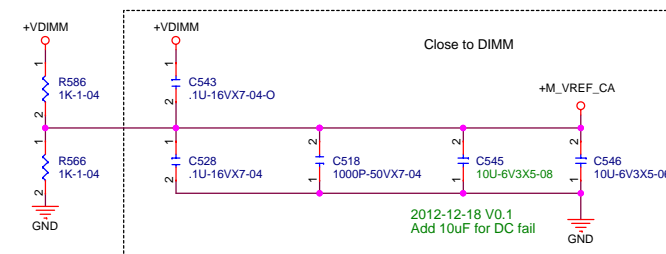
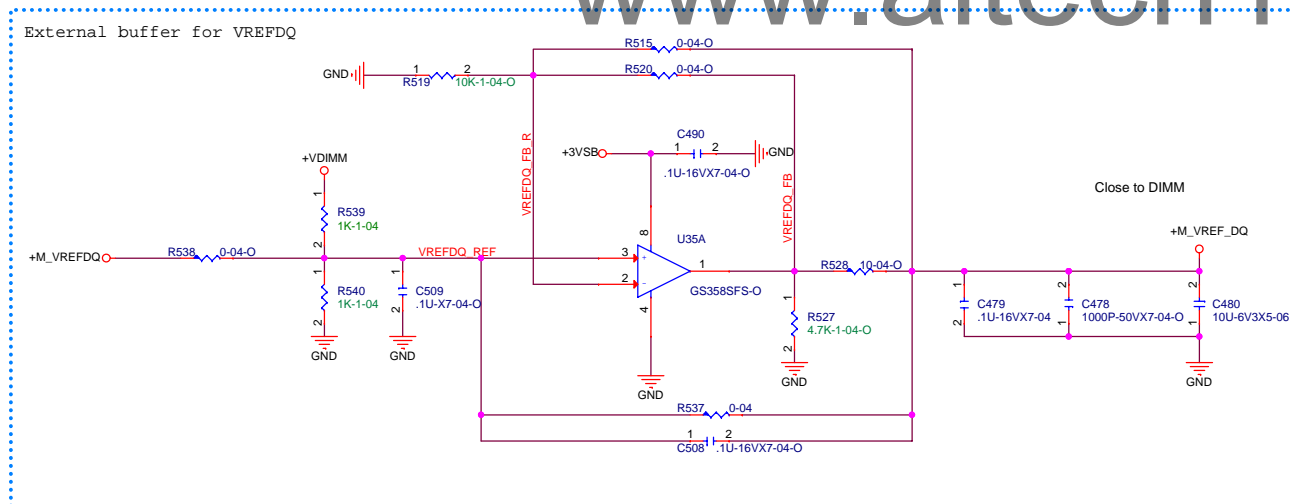
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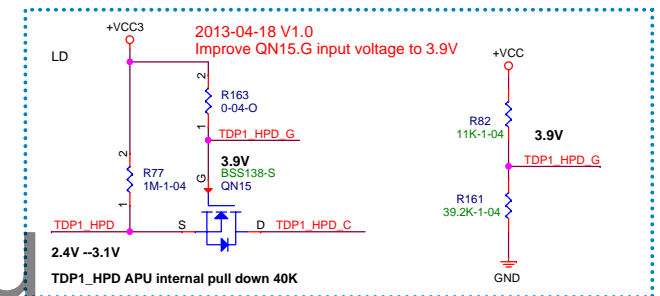
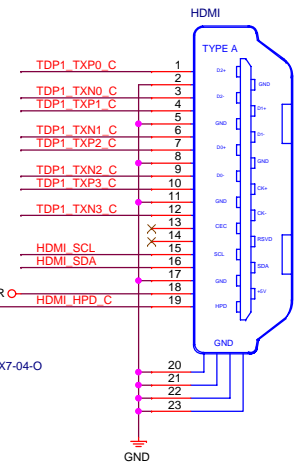
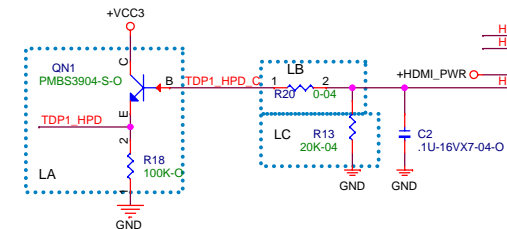
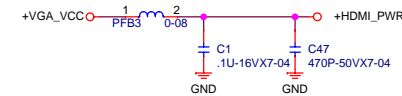
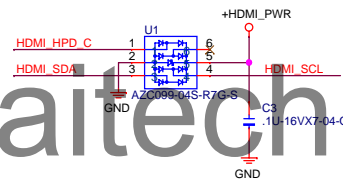
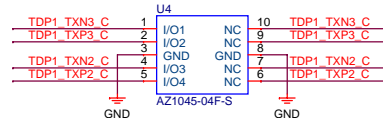
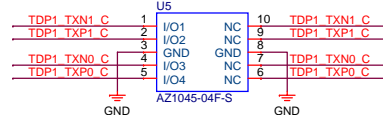
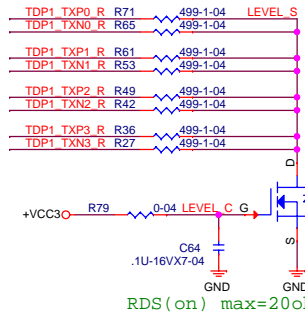
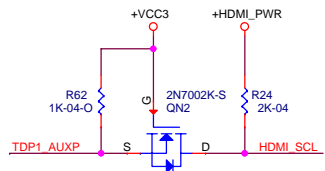
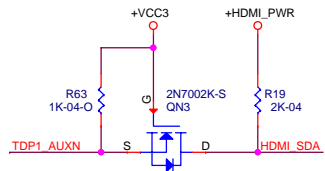
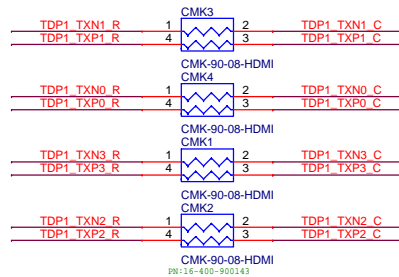
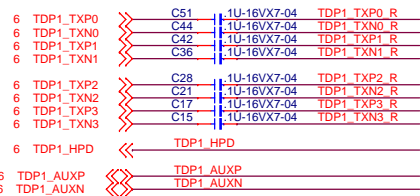






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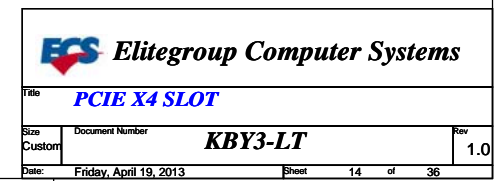
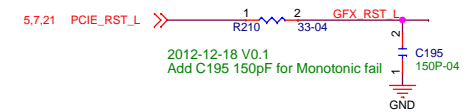


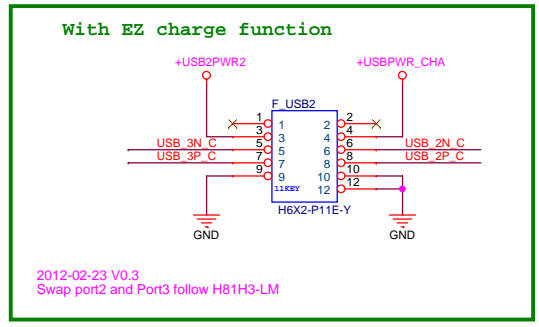
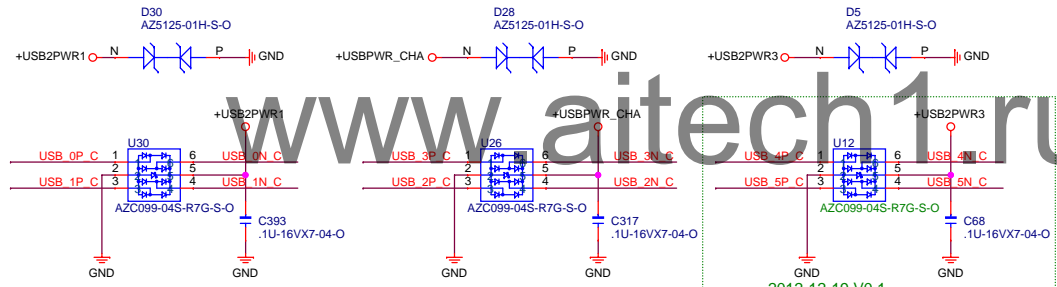
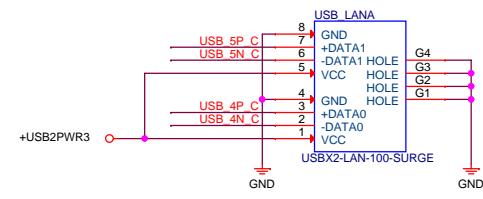
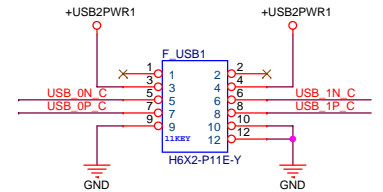
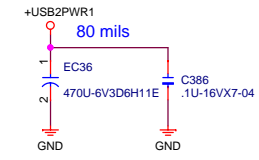
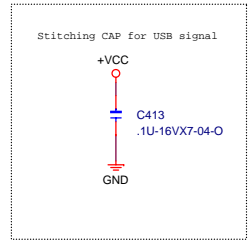
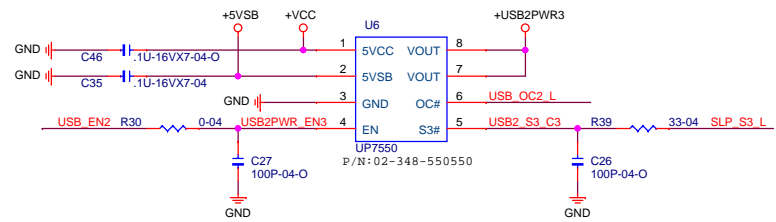
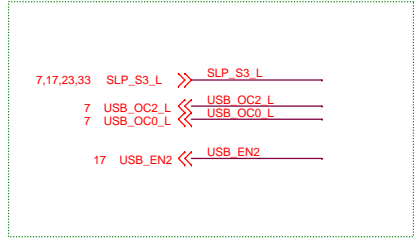
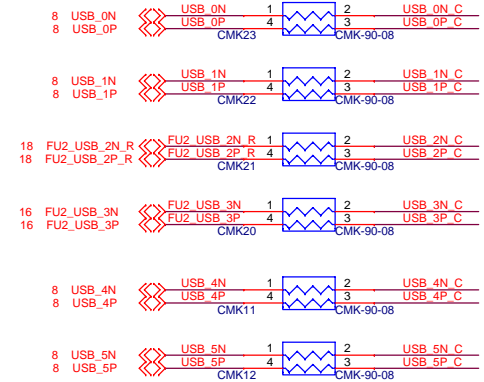


2013-04-18 V1.0  
Improve QN15.G input voltage to 3.9V  
BOM table

	LA	LB	LC	LD
BSS138-S	X	0-04	20K-04	V
PMB3904	V	10K-04	100K-04	X

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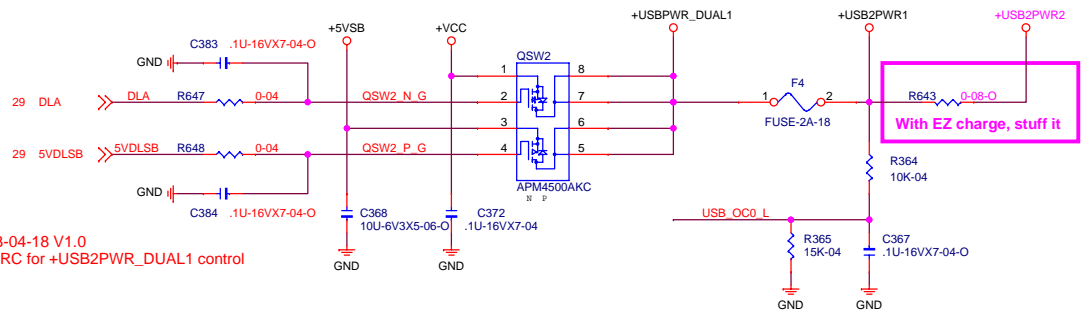




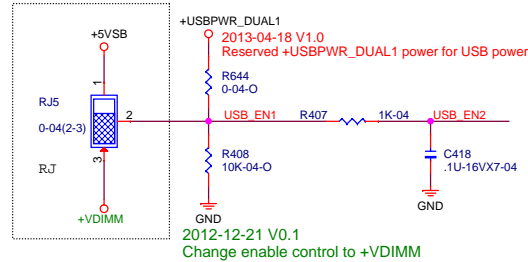
# USB\_DUAL Power

2012-12-19 V0.1  
Remove control circuit, and use DIMM\_DUAL control signal

2013-04-18 V1.0  
Add RC for +USB2PWR\_DUAL1 control



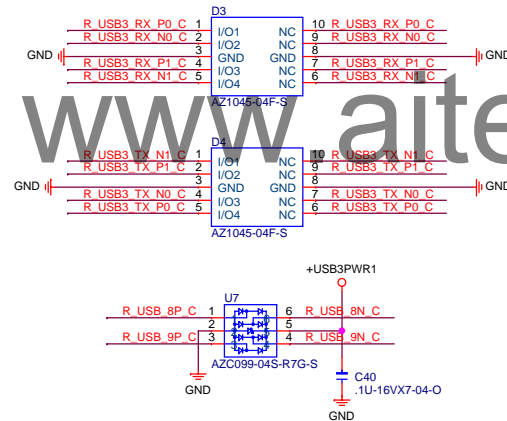
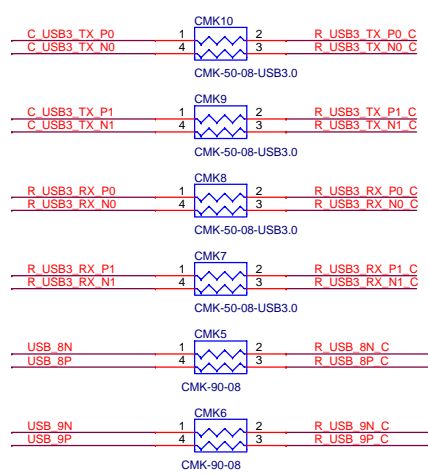
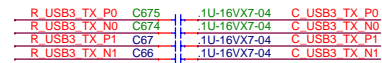
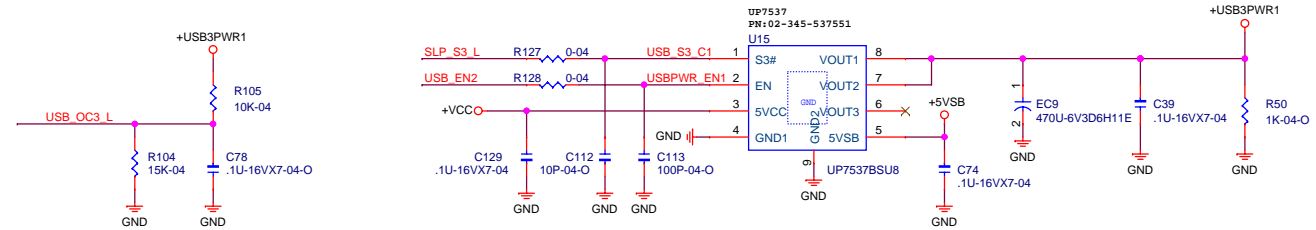
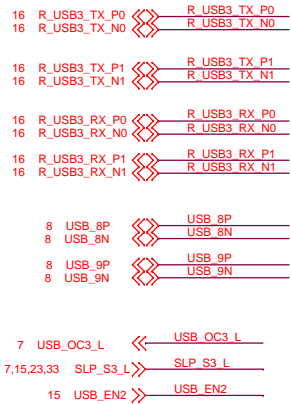
Sleep	DLA	5VDSLBS	+USB2PWR1
S0	1	1	+VCC
S3	0	0	+5VSB
S4/S5	0	1	0



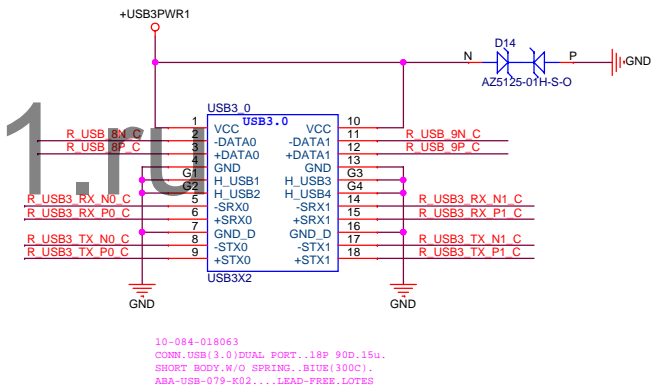
uP7550 Enable use	RJ	S4/S5 USBPWR	Lenovo S4/S5 w/o USB_5V_DUAL
* +VDIMM	0ohm(2-3)	0 Volt	
5VSB	0ohm(1-2)	5 Volt	

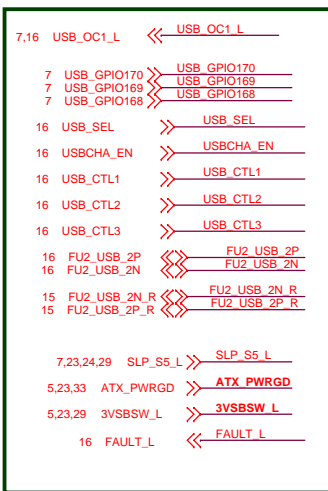




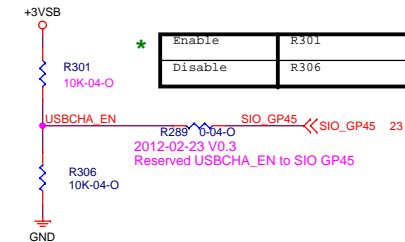
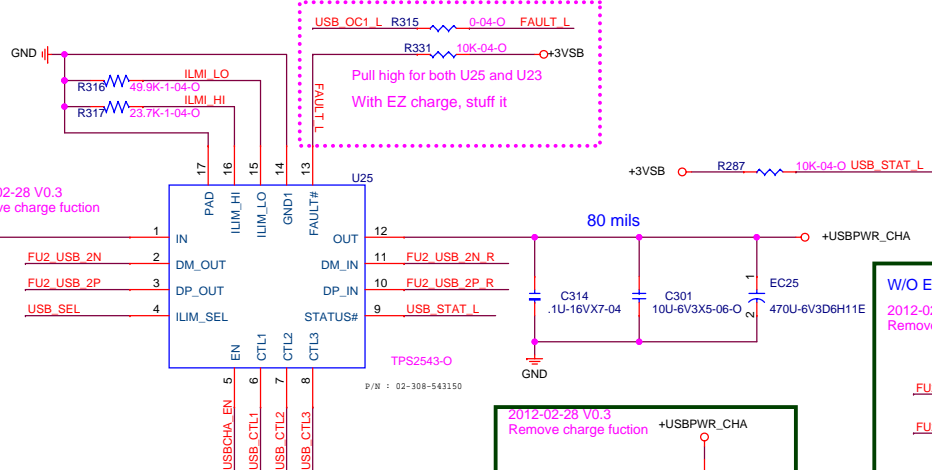


## USB3.0 connector



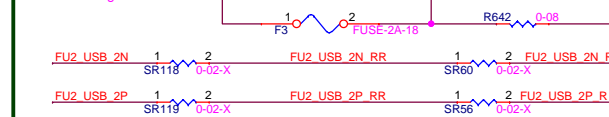


## USB CHARGER

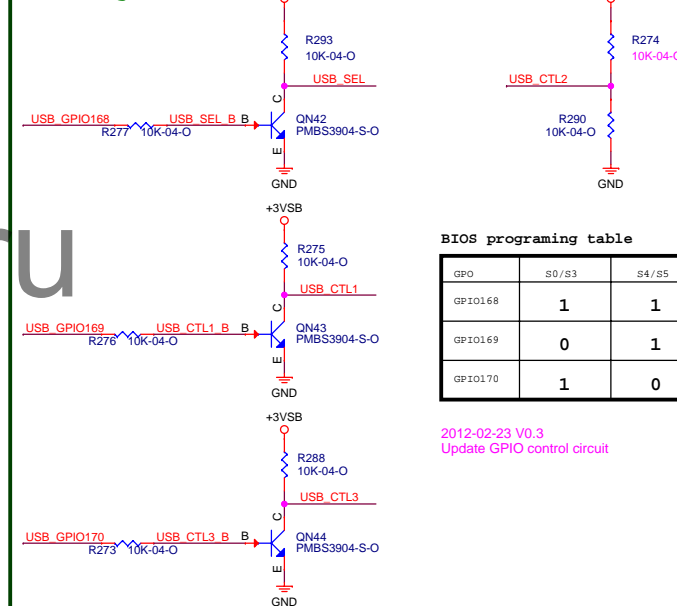


## W/O EZ charge, stuff it

2012-02-28 V0.3  
Remove charge function



## USB Charger GPIO



## BIOS programming table

GPO	S0/S3	S4/S5
GPIO168	1	1
GPIO169	0	1
GPIO170	1	0

2012-02-23 V0.3  
Update GPIO control circuit

## TPS2543 Control Mode

Input Logic Level				Control Mode	
INPUT1	INPUT2	INPUT3	ILIM_SEL	System Status	Charging Mode
0	1	1	0	S4/S5	DCP(Dedicated Charging Port)
1	1	0	0	S0/S3	SDP(Standard Downstream Port)

Note:DCP mode support iPhone 1A, Ipad 2.1A

2012-02-28 V0.3  
Remove charge function  
2012-12-17 V0.1  
Change control signal for +USBPWR\_DUAL  
power drop issue when S3 to S0

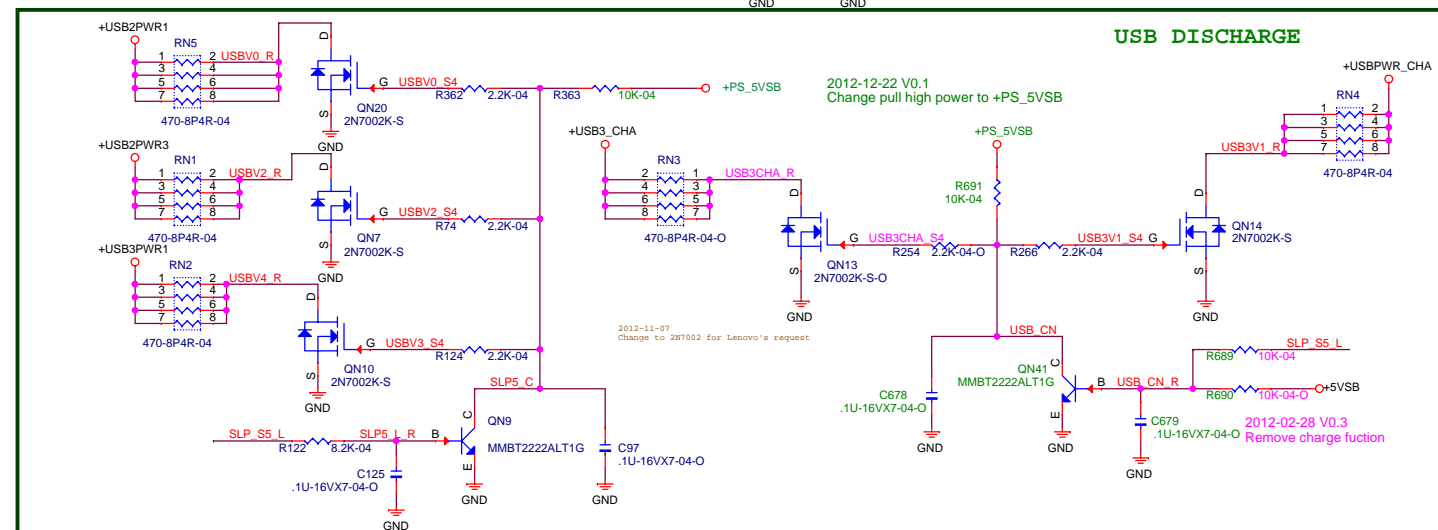
## W/O EZ charge, stuff it

3VBSW\_L R337 10K-04

## ATX\_PWRGD R327 10K-04-O

With EZ charge, stuff it

2012-02-23 V0.3  
Change ATX\_PWRGD pull high to 4.7K

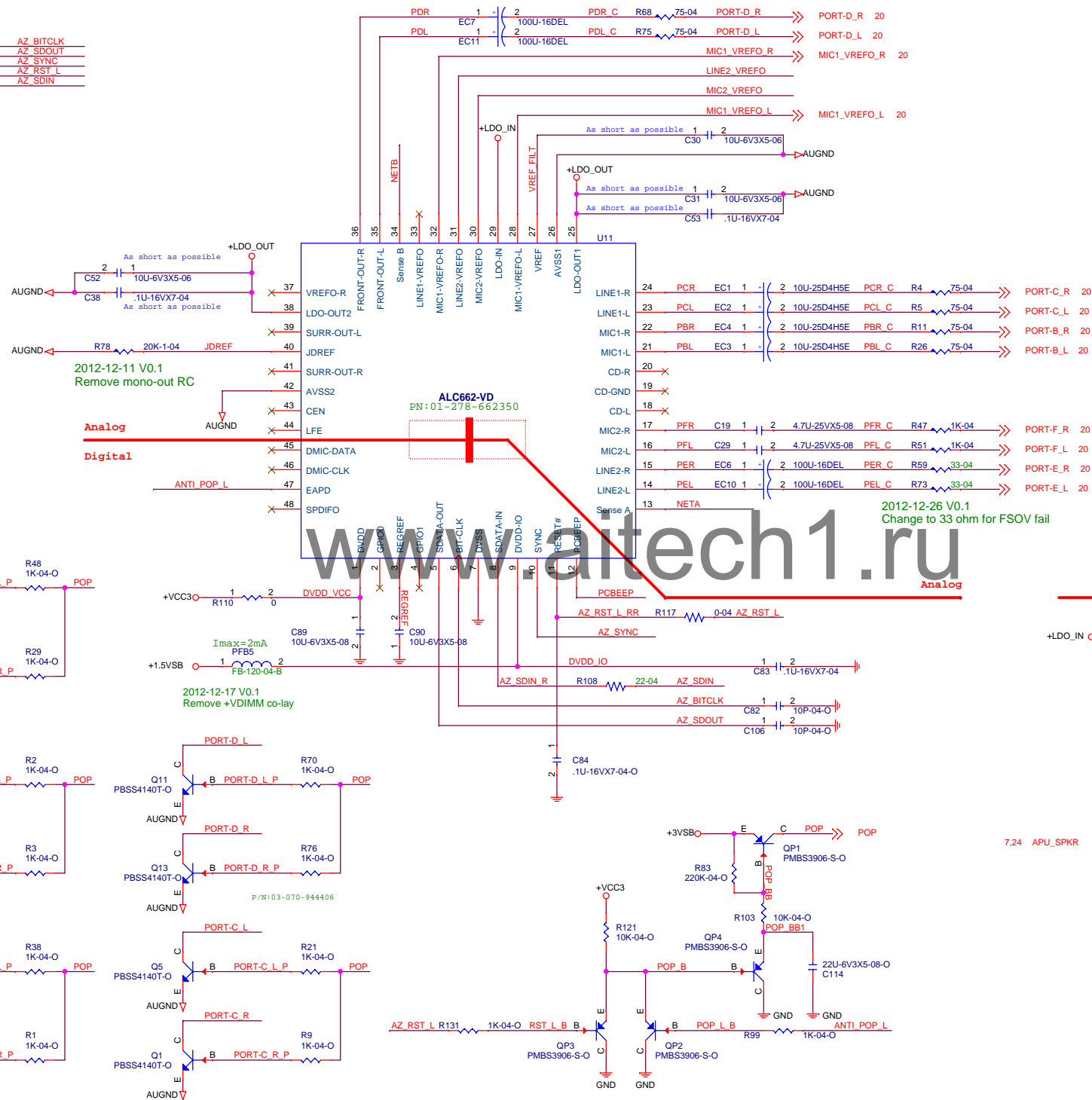


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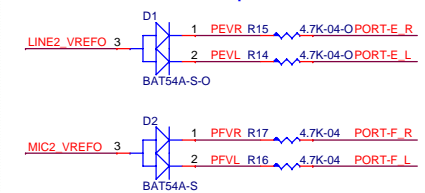
USB EZ CHARGER

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7 AZ\_BITCLK >>> AZ\_BITCLK  
7 AZ\_SDOOUT >>> AZ\_SDOOUT  
7 AZ\_SYNC >>> AZ\_SYNC  
7 AZ\_RST\_L >>> AZ\_RST\_L  
7 AZ\_SDIN >>> AZ\_SDIN

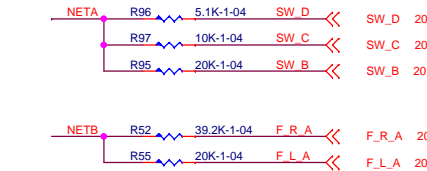


#### Verfourt bias for stereo microphone.

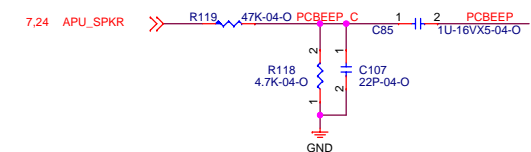
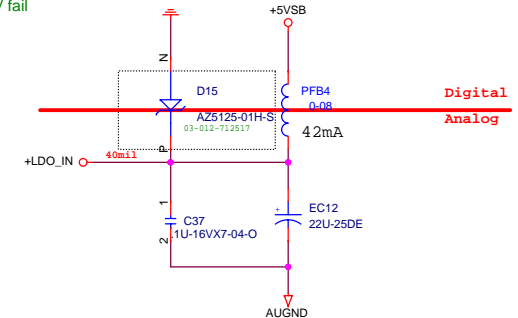


Placement near to codec

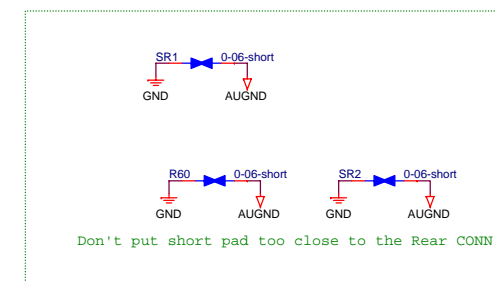
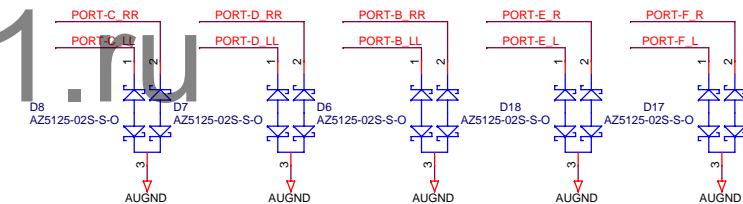
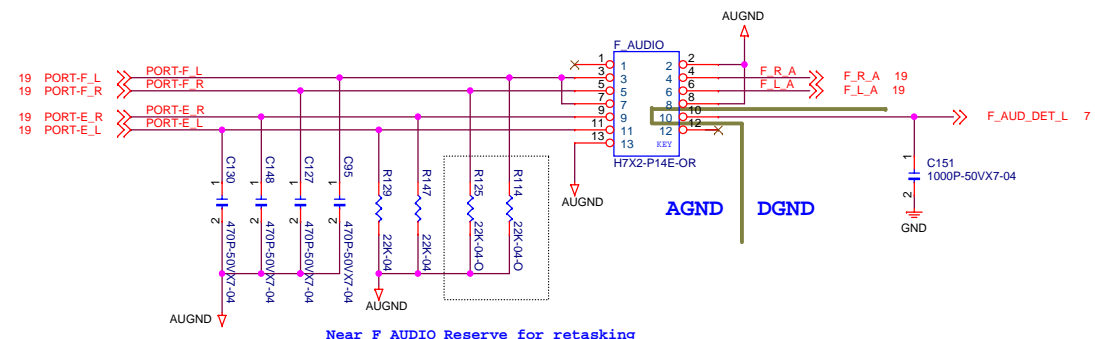
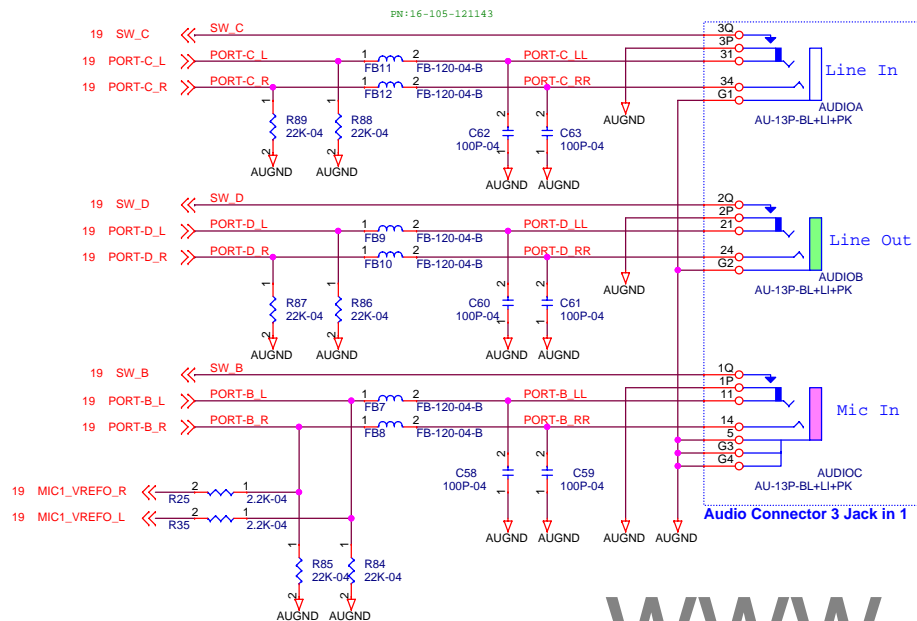
#### Resistors Networks



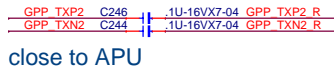
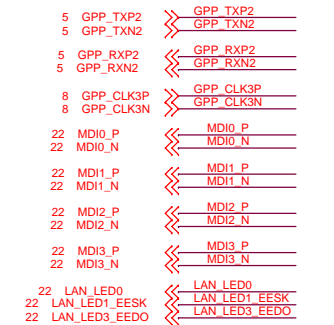
Placement near to codec



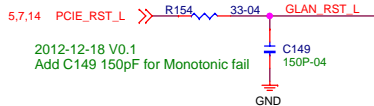
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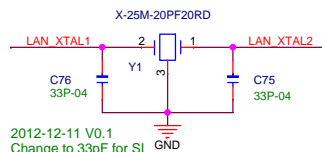
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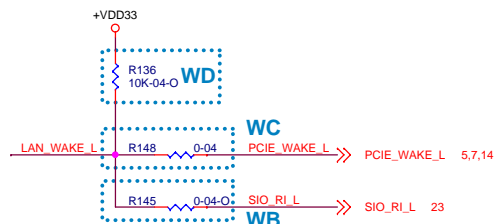
close to LAN



Crystal Spec:  $\pm 30\text{ppm}$ ,  $CL=20\text{pF}$   
 $Ce=2 \cdot CL \cdot (Cs+Ci)$

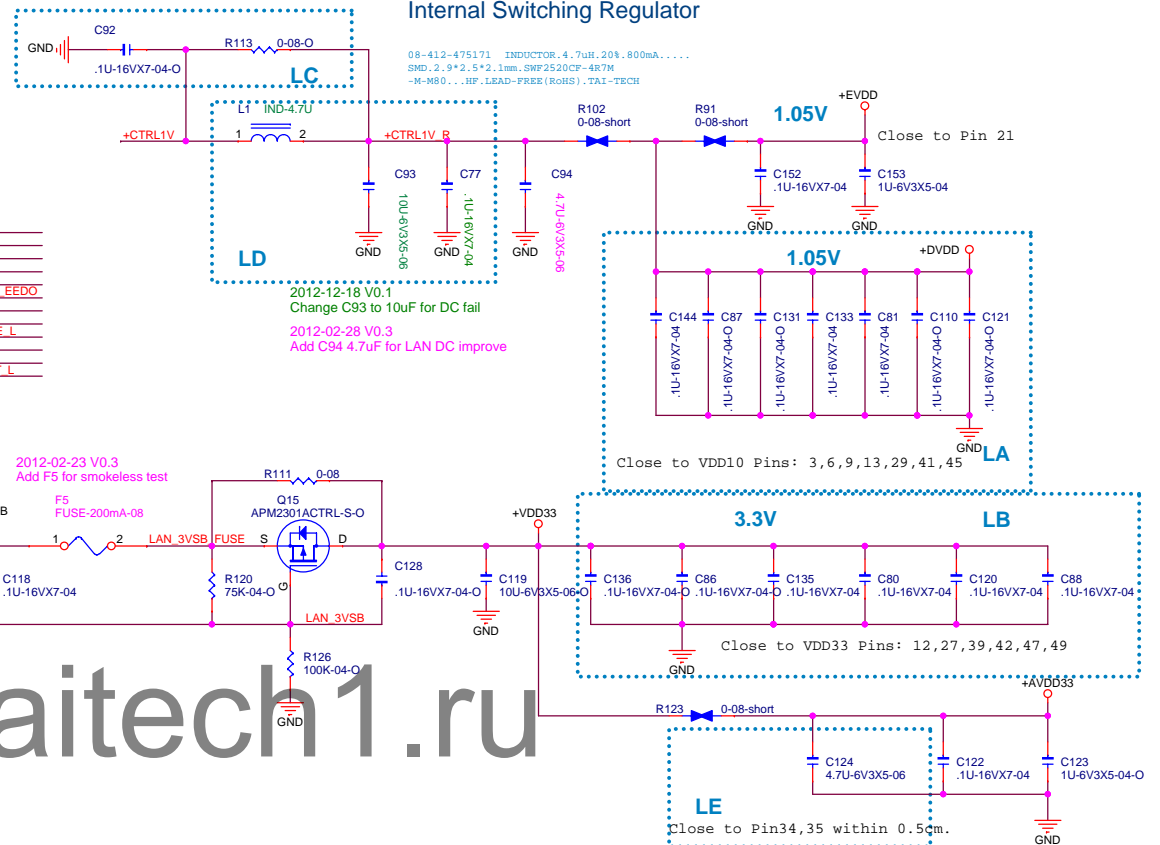
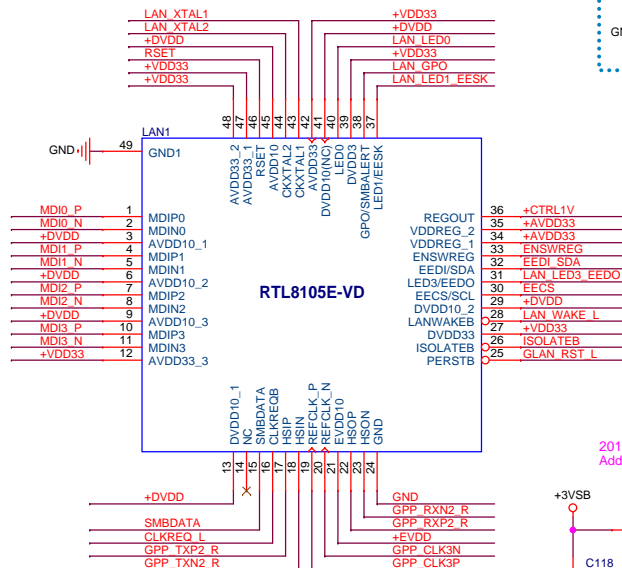


2012-12-11 V0.1  
 Change to 33pF for SI



For WOL option

MODE	WB	WC	WD
WOL Normal	X	V	X
WOL G3->S5	V	X	V
WO_PCIEs G3->S5	V	V	X



01-267-105353

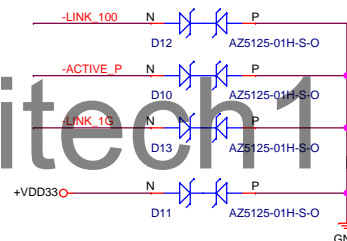
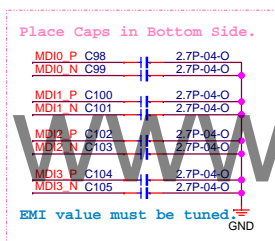
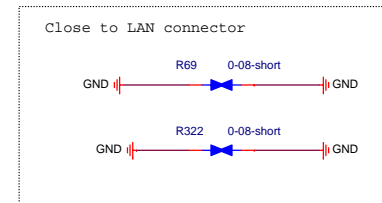
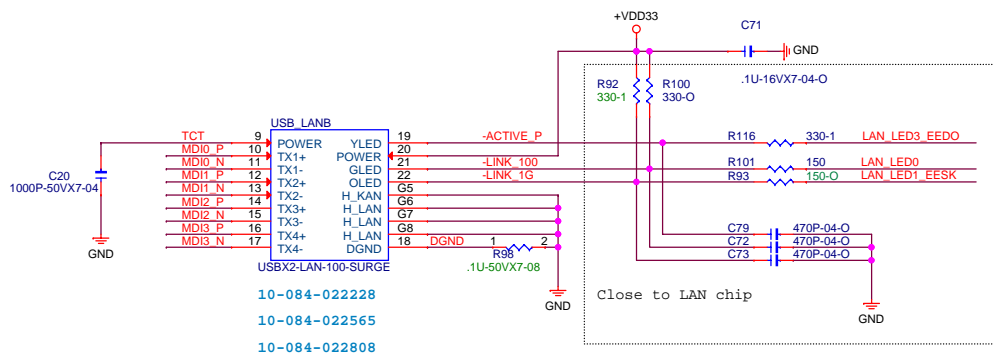
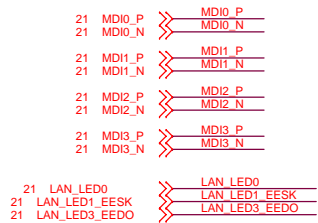
01-267-106351

Chip/Version	LA	LB	LC	LD	LE	LF
RTL8105E-VD *	3PCS(pin13,29,45)	4PCS(pin27,39,47,48)	X	V	V	V
RTL8106EN-CG	2PCS(pin9,45)	3PCS(pin35,47,48)	V	X	X	X

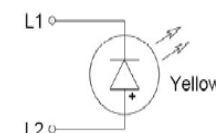
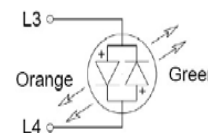
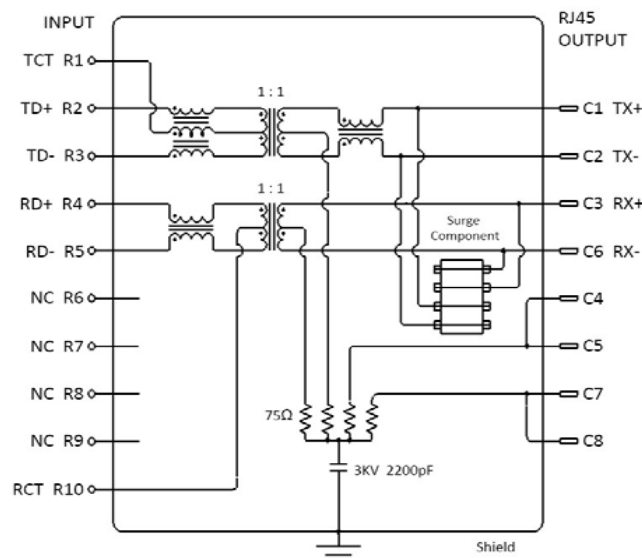
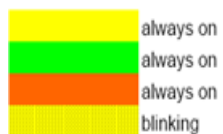
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**LAN-RTL8105E-VD\_RTL8106EN-CG**

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 Date: Friday, April 19, 2013 Sheet: 21 of 36

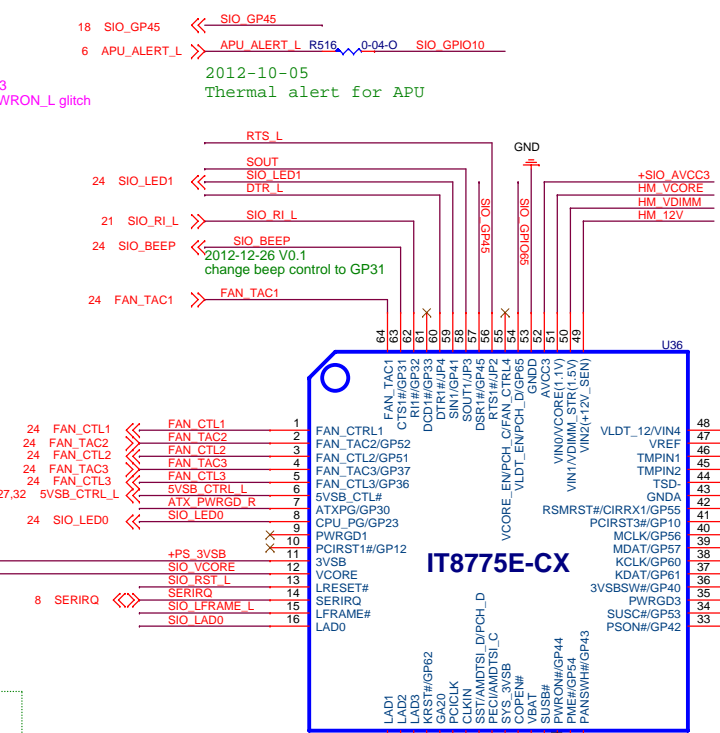
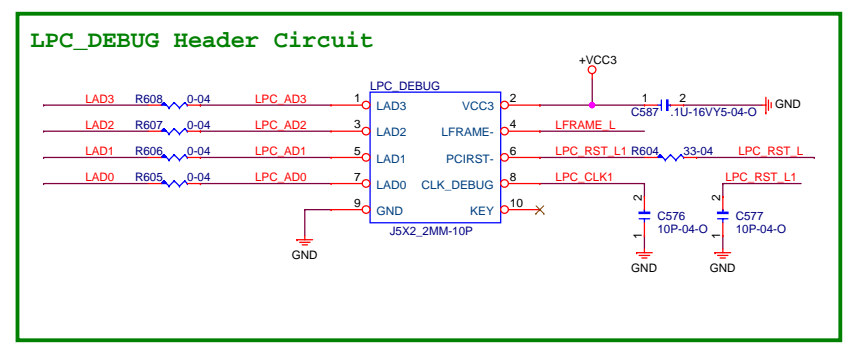
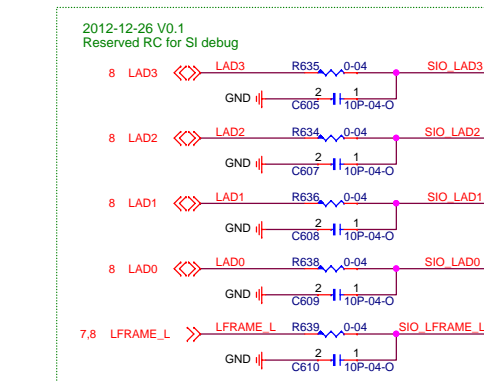
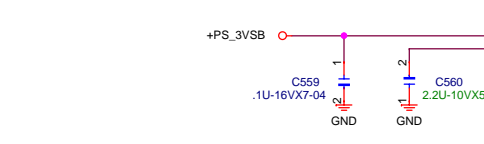
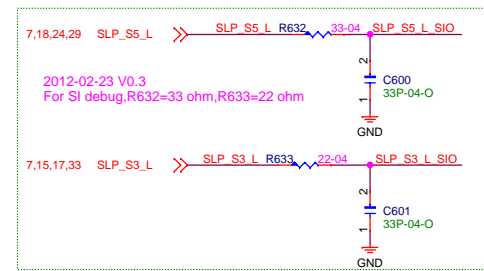
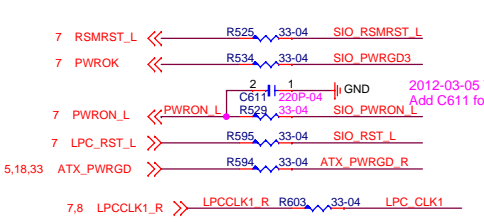


WOL	status	Yellow	Gm/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

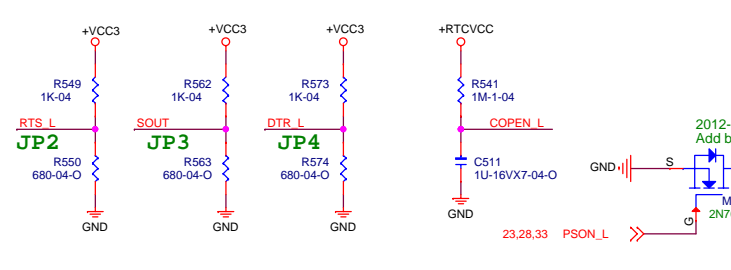


Emitting Color	λp (nm)	Vf @If=20mA	Ir @Vr=5V
Green	565	1.7~2.6 V	10μA max.
Yellow	585	1.7~2.6 V	10μA max.
Orange	610	1.7~2.6 V	10μA max.



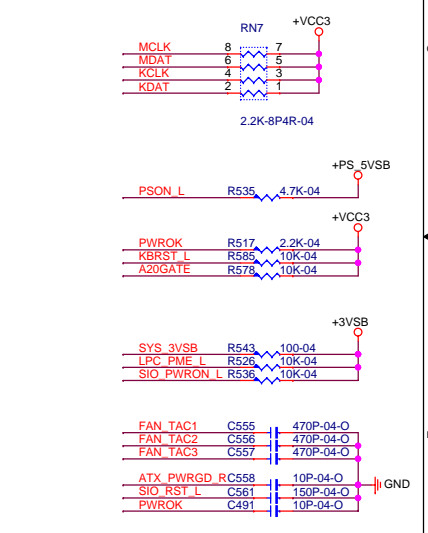
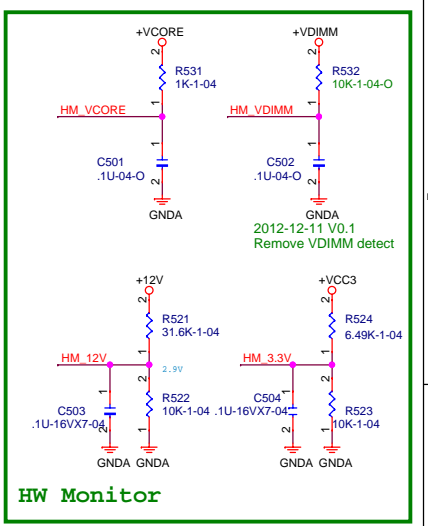
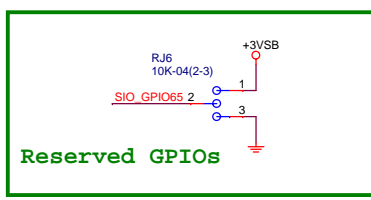


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**IT8775F Power On Strapping Options**

Symbol	value	Description
JP4	1	K8 power sequence function is disabled
Pin 60	0	K8 power sequence function is enabled
JP3 & JP5	11	The default value of EC Index 15h/16h/17h is 80h
Pin 58 & 21	10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
	01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
	00	The default value of EC Index 15h/16h/17h is 40h
JP2	1	Disable WDT to rest PWROK
Pin56	0	Enable WDT to rest PWROK

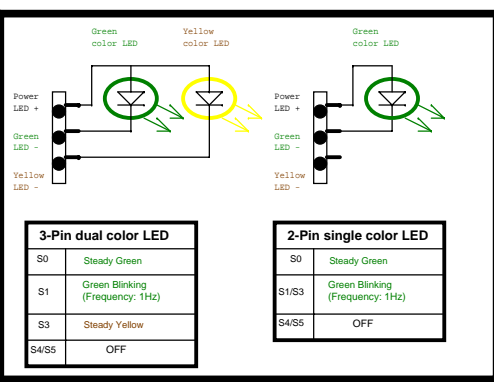
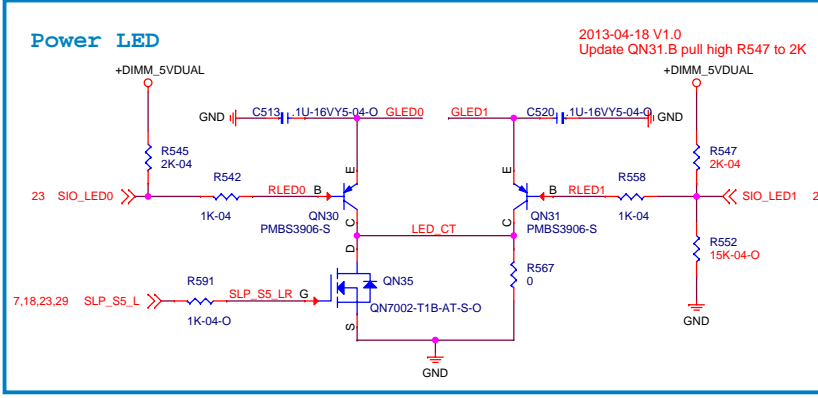
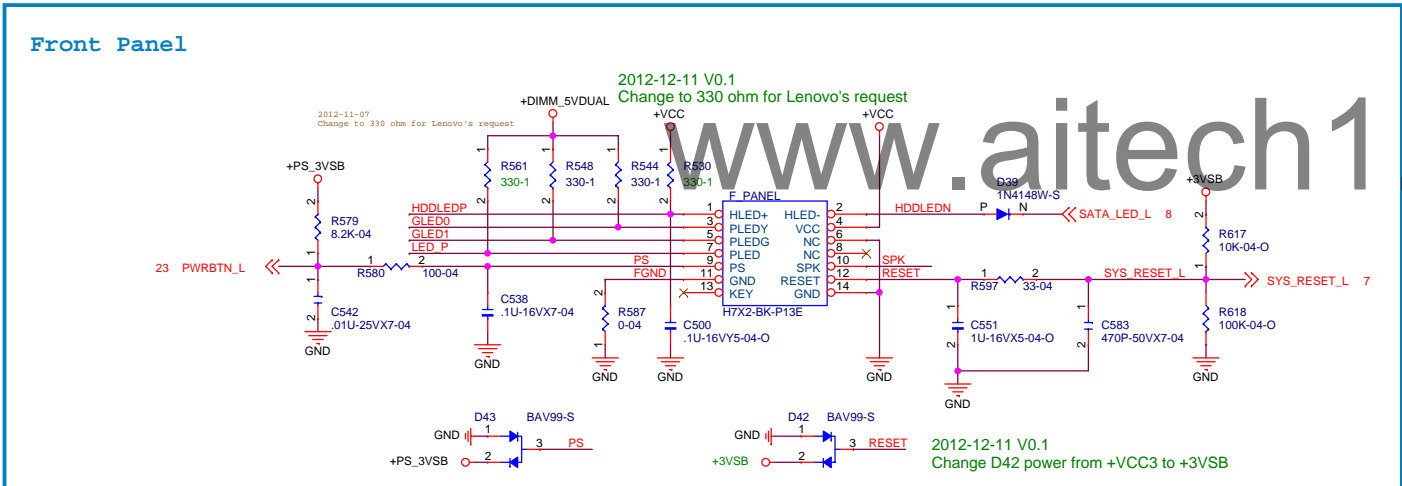
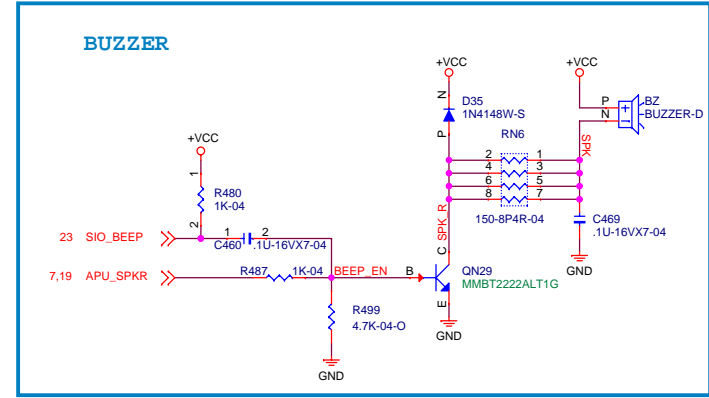
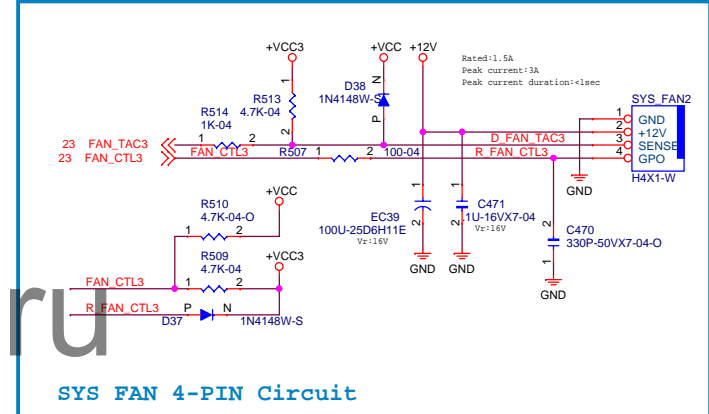
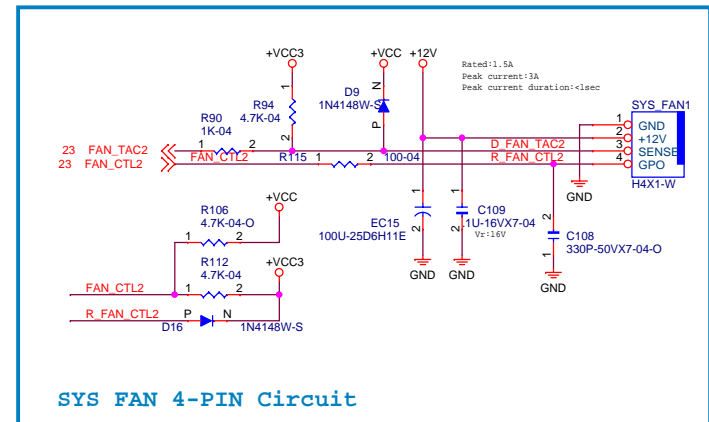
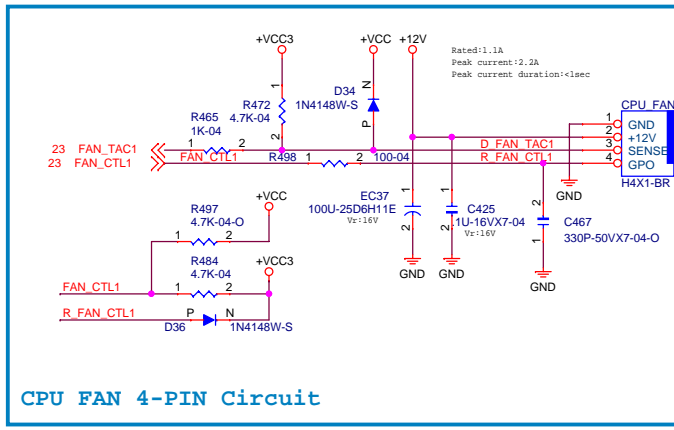
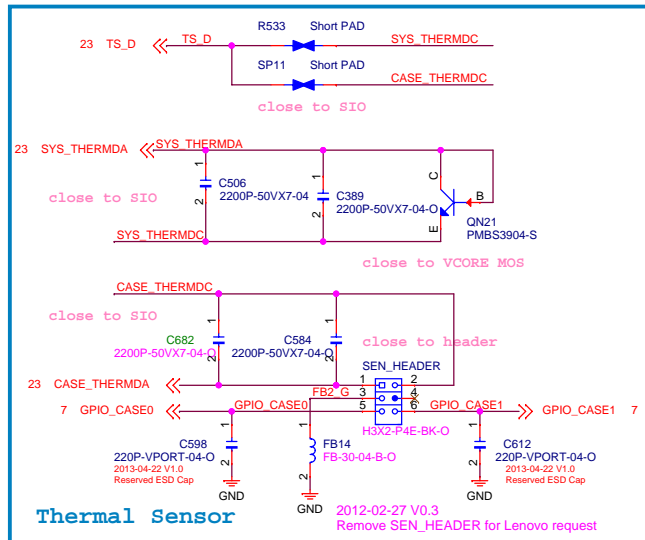


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**SIO-IT8775E-CX**

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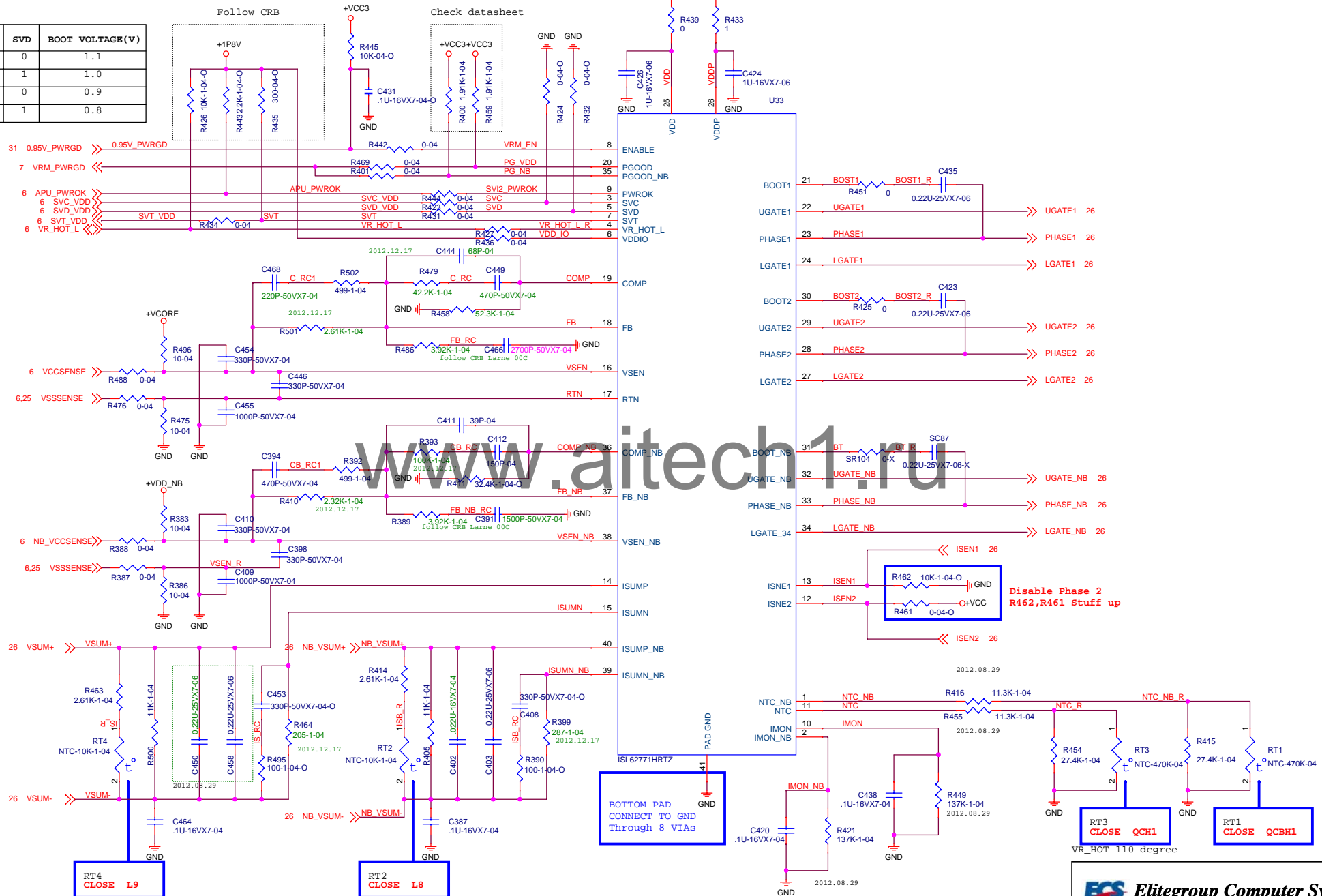


**Lenovo LED線路阻値330-06**

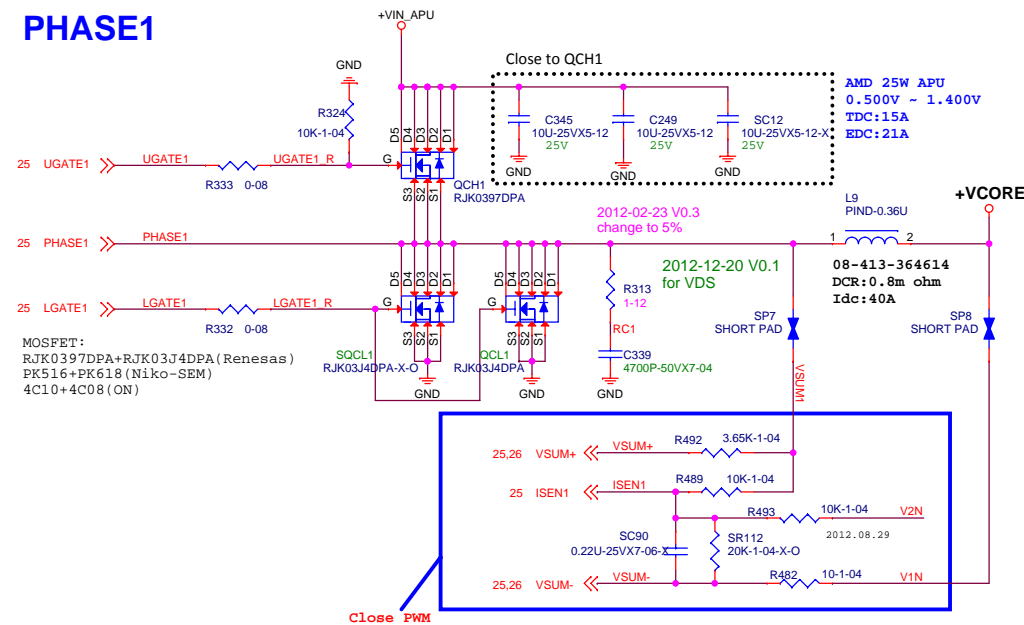
Source Voltage (V)	5
LED Forward Voltage (V)	1.8
BJT Vce(s) (V)	0
Pull Up Resistor (ohm)	330
LED Forward Current (A)	0.009697
Pull Up Resistor Power (R<1/10 W)	0.03103
LED Power (W)	0.017455

# ISL62771 Schematic for FT3 solution

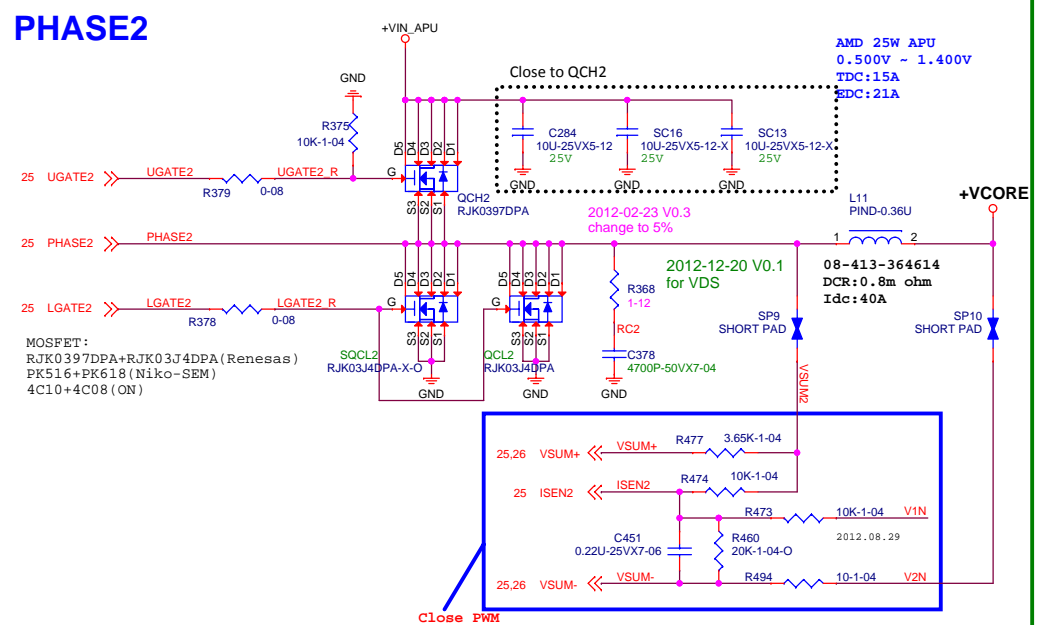
SVC	SVD	BOOT	VOLTAGE(V)
0	0	1.1	
0	1	1.0	
1	0	0.9	
1	1	0.8	



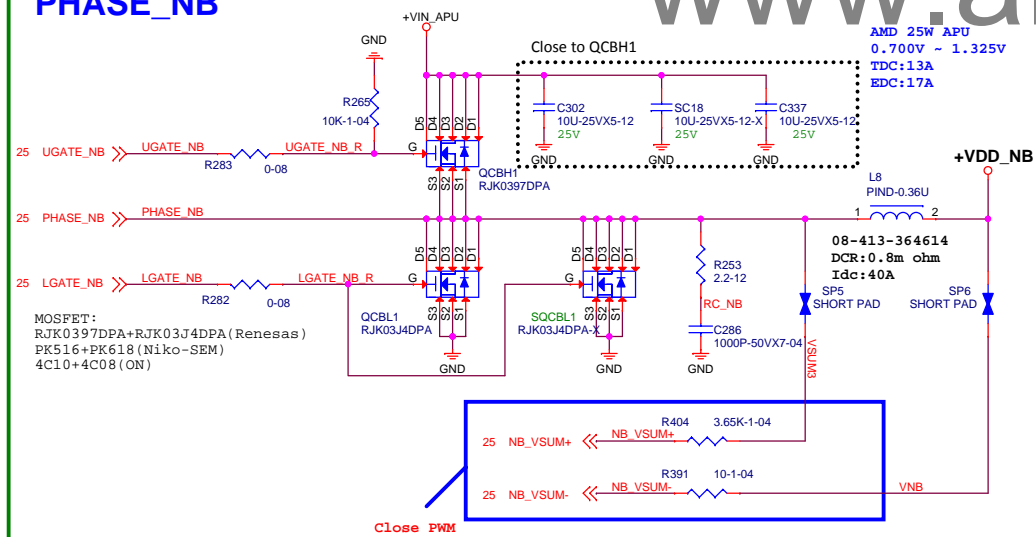
## PHASE1



## PHASE2

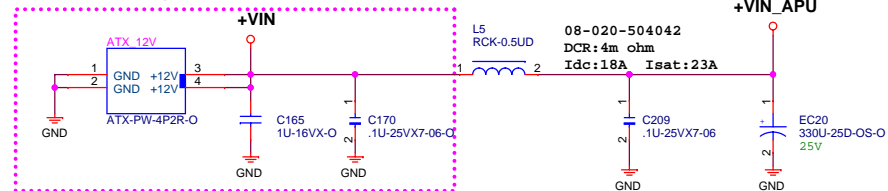


## PHASE\_NB

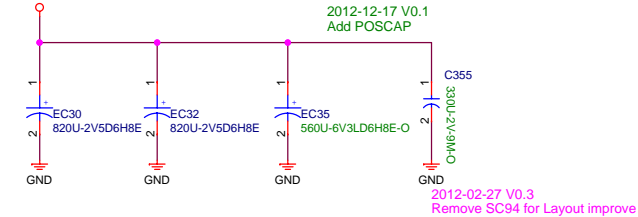


## ATX 4P

### ATX Solution Stuff Up



### +V CORE



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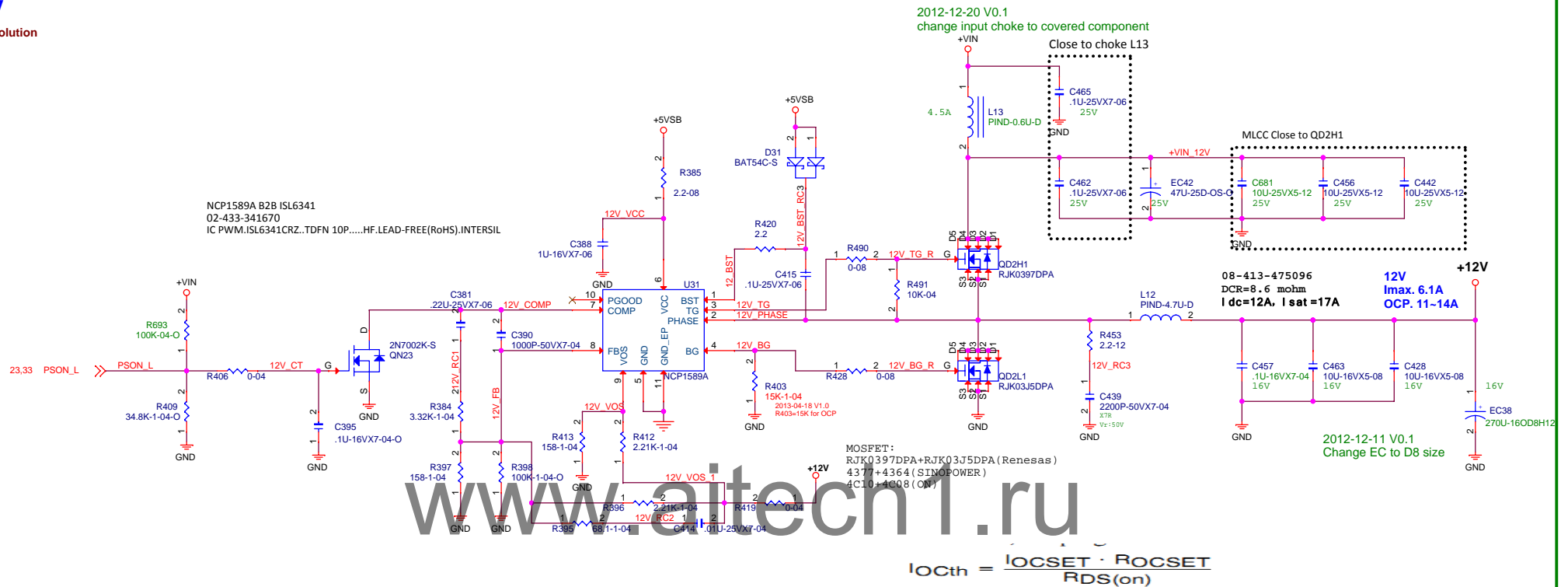
**+V CORE +NBCORE2**

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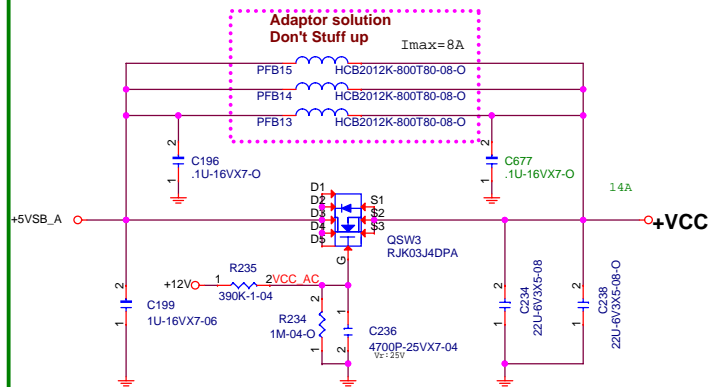
## Adaptor solution

### Stuff up

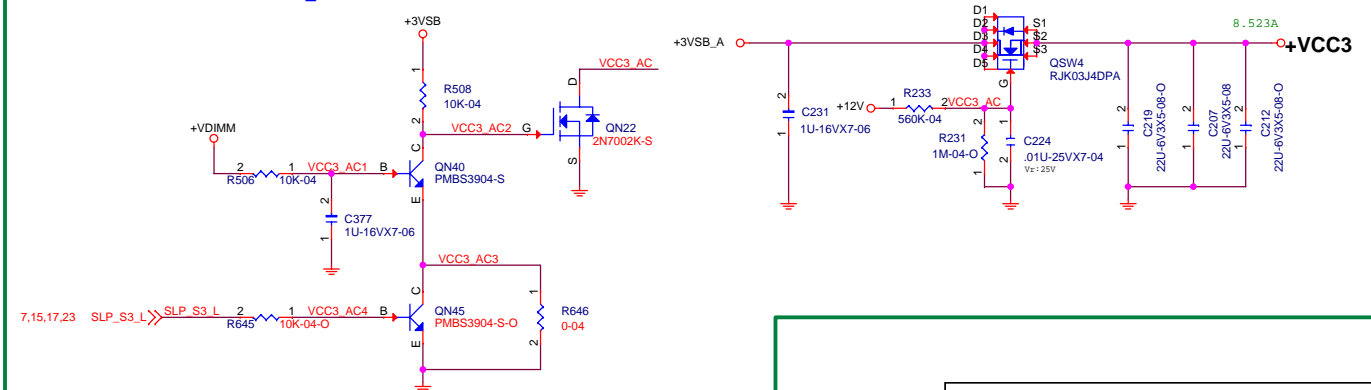


$$I_{OCth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}}$$

## +VCC

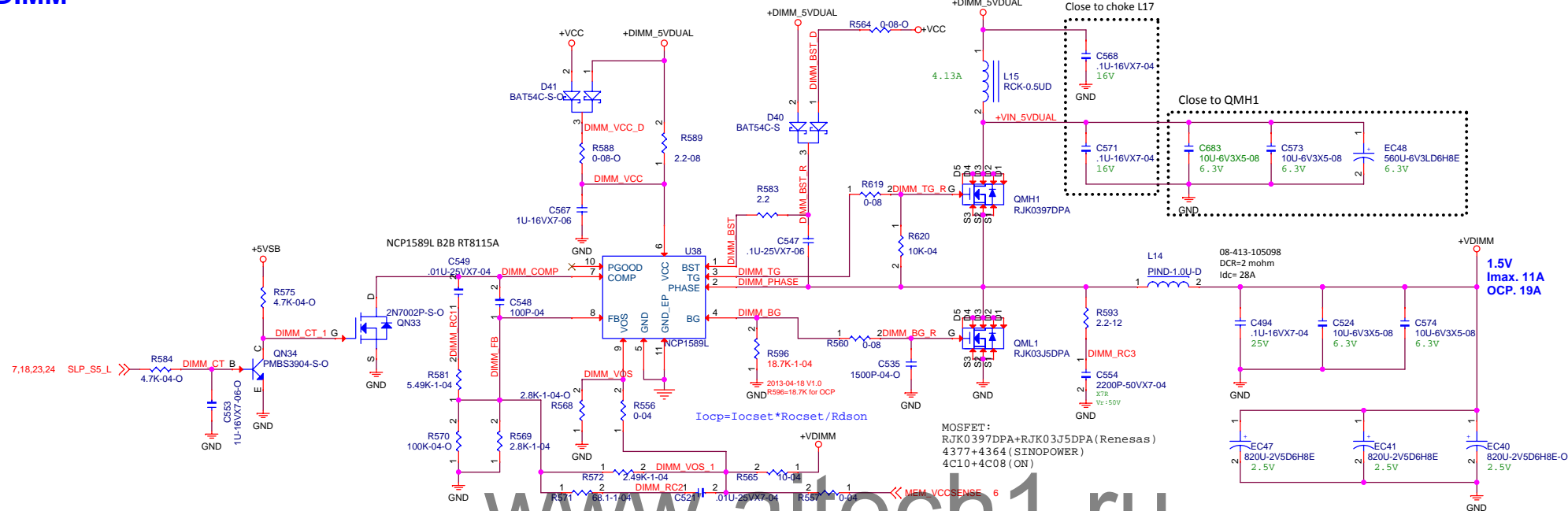


## +VCC3 delay control

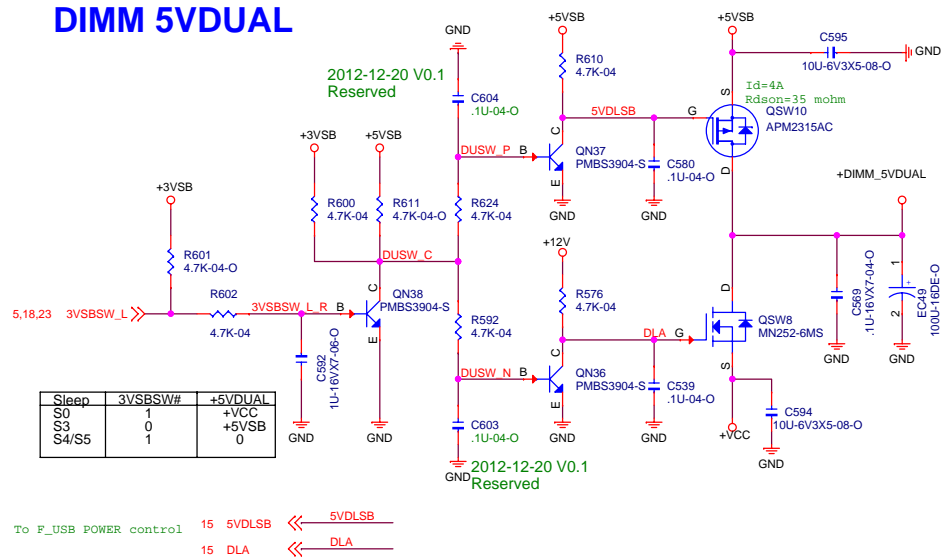


2012-12-20 V0.1  
Add +VCC3 delay circuit follow AMD Group C and D sequence  
2013-04-18 V1.0  
Add SLP\_S3 control +VCC3 power down, QN22 change to 2N7002

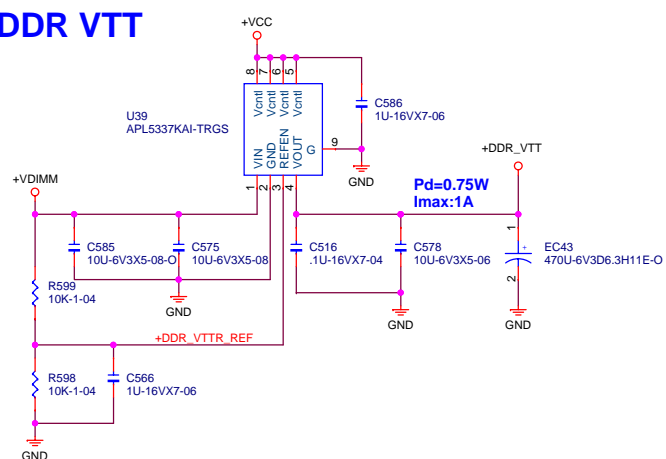
## VDIMM



## DIMM 5V DUAL

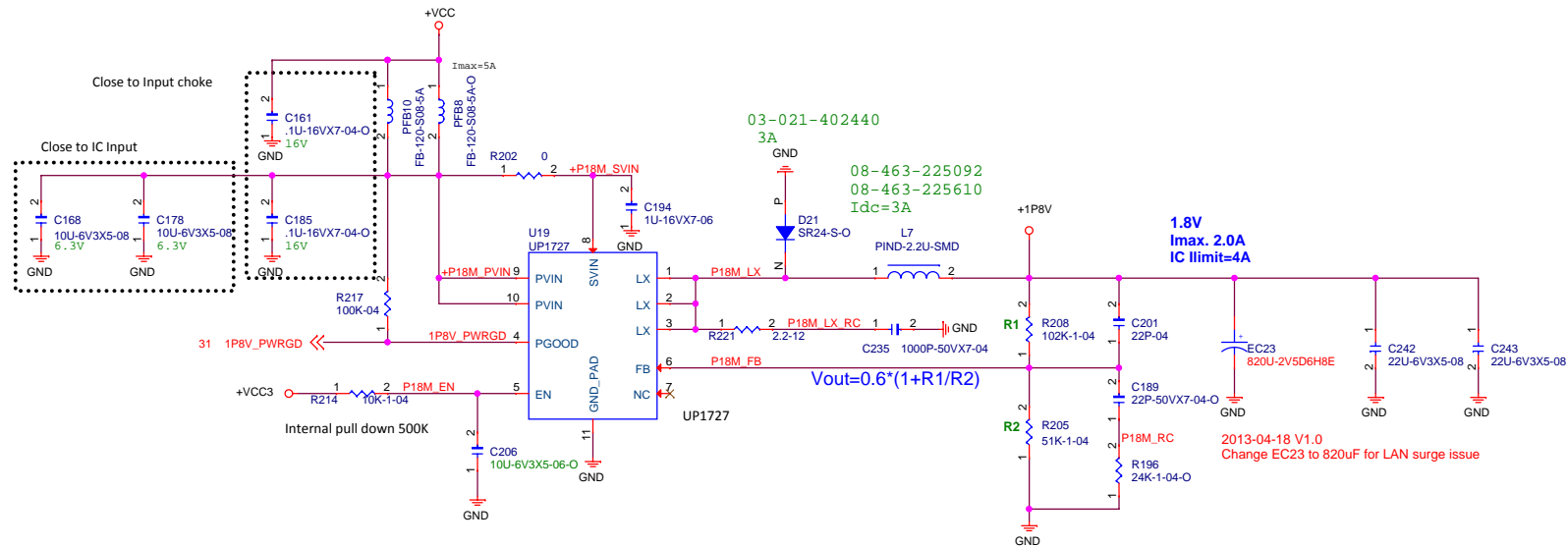


## DDR VTT



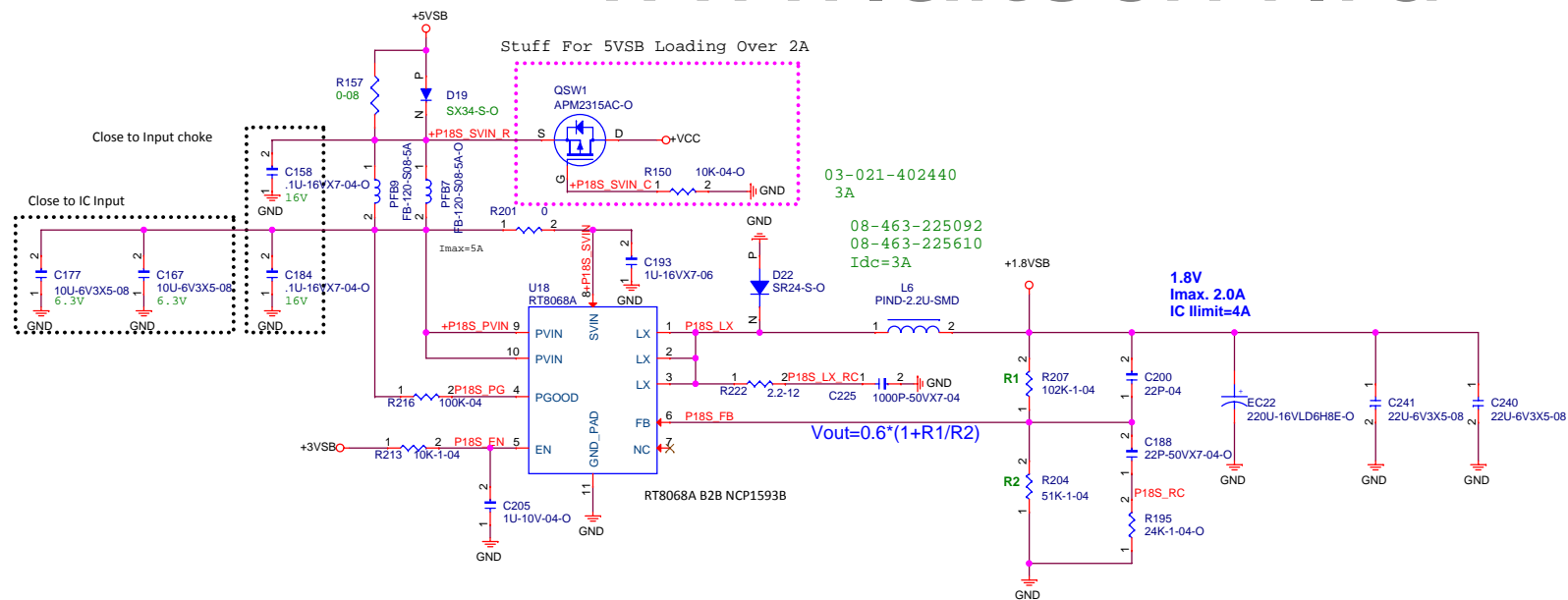


# 1P8V



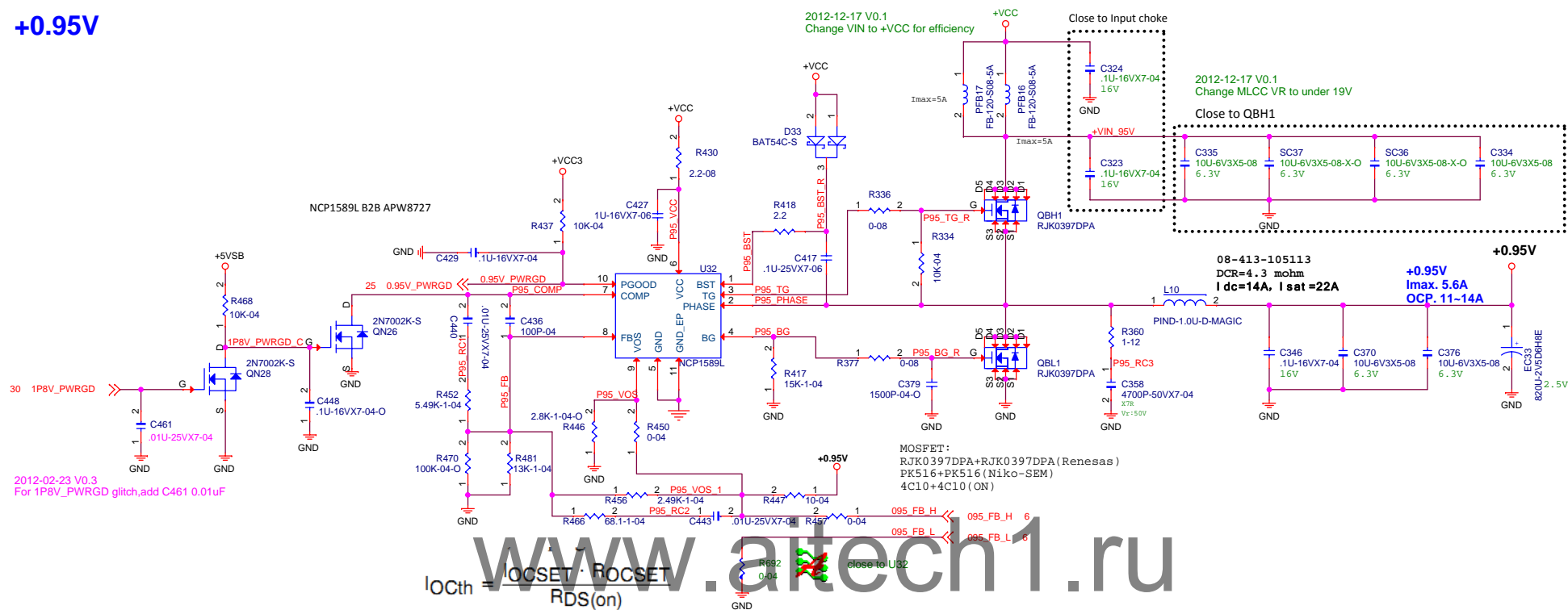
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# 1.8VSB

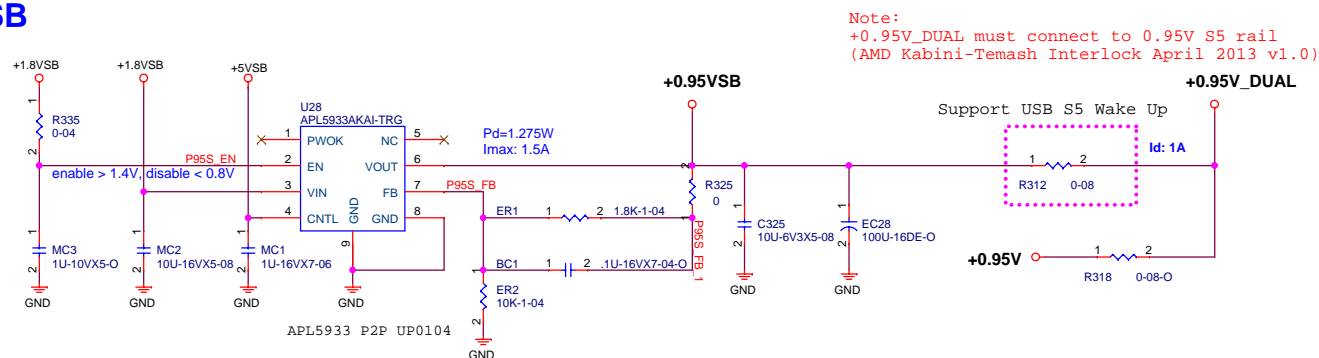


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**+0.95V**



**0.95VSB**



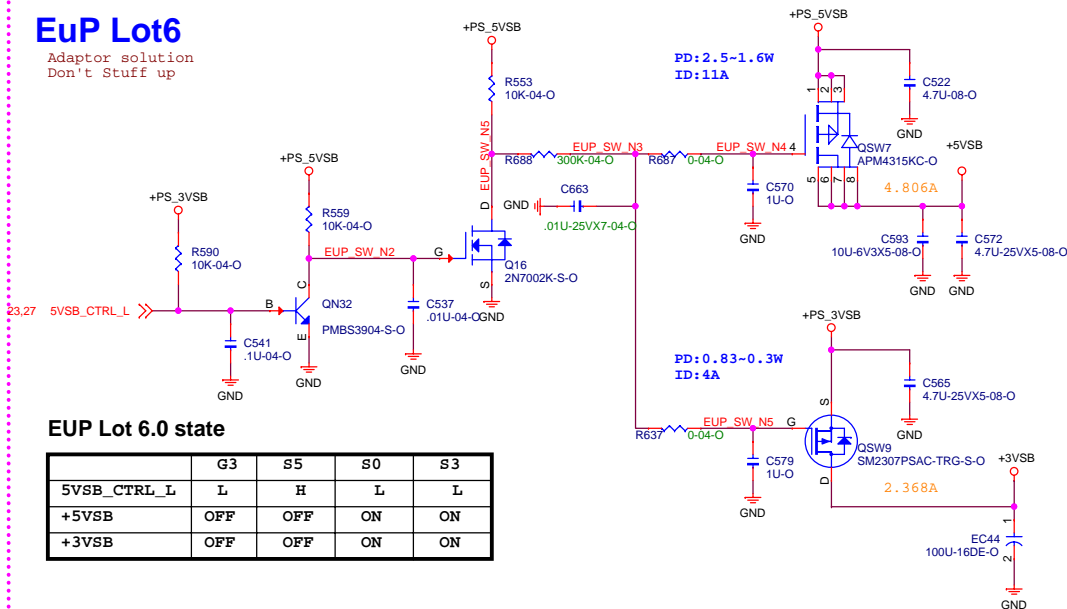
Note:  
+0.95V\_DUAL must connect to 0.95V S5 rail  
(AMD Kabini-Temash Interlock April 2013 v1.0)

Support USB S5 Wake Up

**+0.95V** 

## EuP Lot6

Adaptor solution  
Don't Stuff up

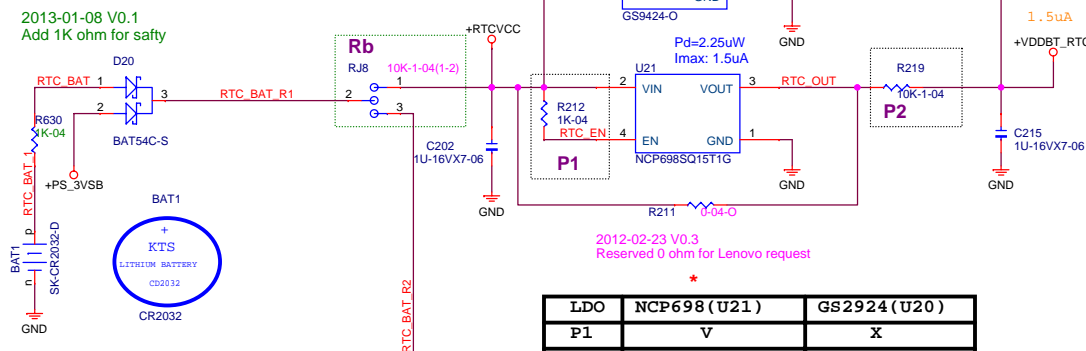


### EUP Lot 6.0 state

	G3	S5	S0	S3
5VSB_CTRL_L	L	H	L	L
+5VSB	OFF	OFF	ON	ON
+3VSB	OFF	OFF	ON	ON

## VDDBT\_RTC

2013-01-08 V0.1  
Add 1K ohm for safety



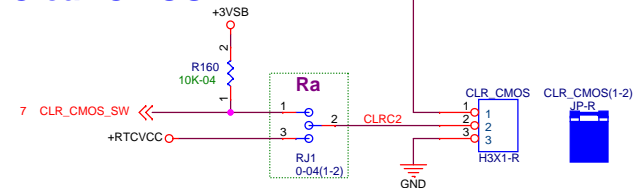
2012-02-23 V0.3  
Reserved 0 ohm for Lenovo request

LDO	NCP698 (U21)	GS2924 (U20)
P1	V	X
P2	V	X

02-346-698030

02-348-924811

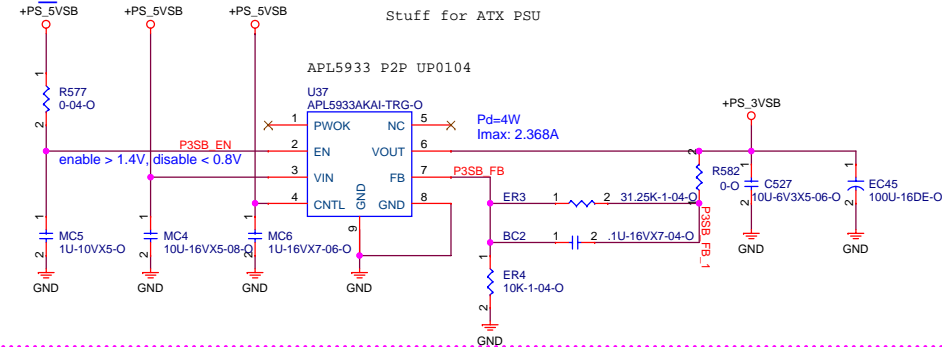
## Clear CMOS



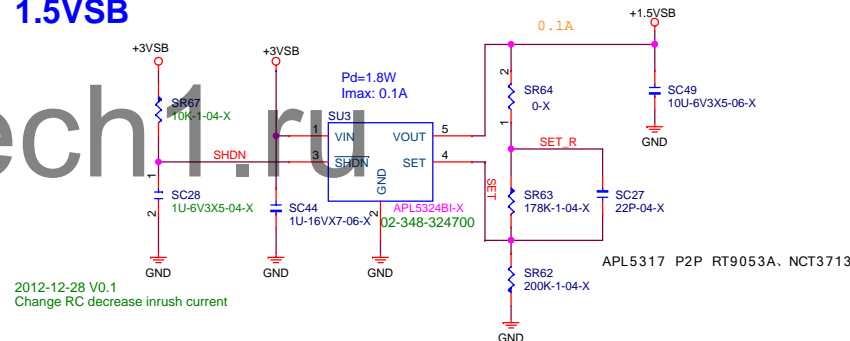
CLR_CMOS	Ra	Rb
1-2	NORMAL	
2-3	CLEAR	

CLR_CMOS	Ra	Rb
SW CLR	(1-2)	(1-2)
HW CLR	(2-3)	(2-3)

## PS 3VSB



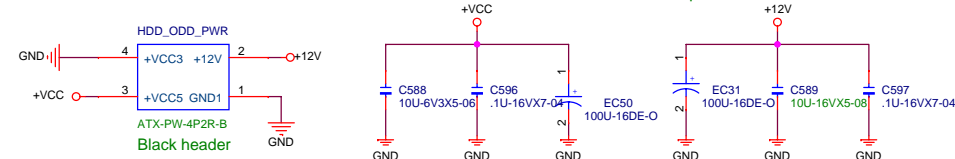
## 1.5VSB



2012-12-28 V0.1  
Change RC decrease inrush current

## HDD/ODD POWER

2012-12-11 V0.1  
Reserved EC for HDD power



2012-02-23 V0.3  
Change pin4 to GND for Lenovo request

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File: **+PS\_3VSB\_+1.5VSB\_EUP\_CIR\_CMOS\_HDD\_PWR**

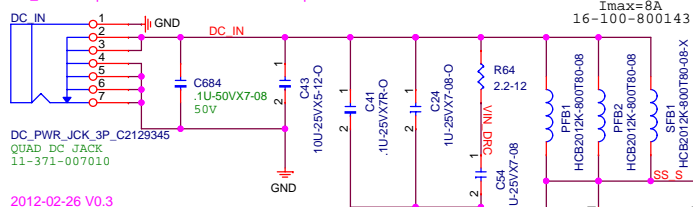
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## DC\_IN 19V

### Adaptor Solution Stuff Up

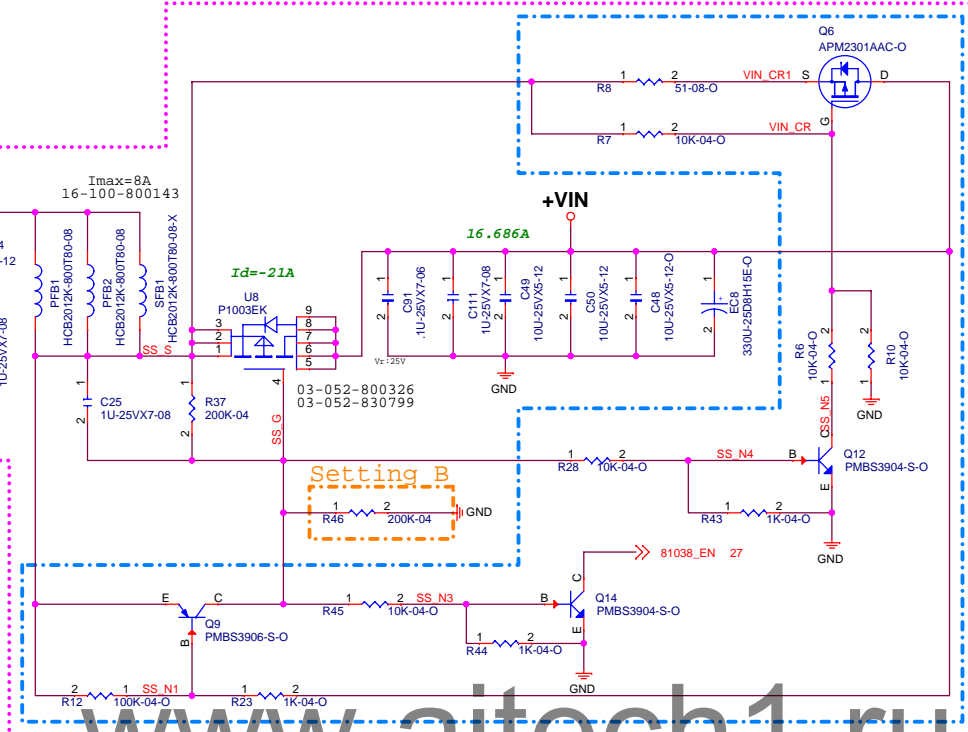
2012-02-26 V0.3  
DC\_IN detect pin connect to GND for Lenovo request



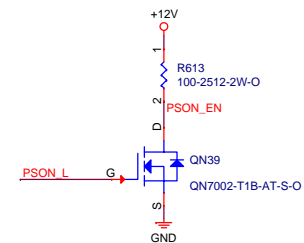
2012-02-26 V0.3  
Update DC\_IN footprint to SMD phase

2013-04-18 V1.0  
Update DC\_IN footprint to DC\_POWER\_JACK\_7P-TE\_2, change to DIP phase

	Original Soft Start Circuit	Limit Current Soft Start Circuit
Setting_A	Non-Stuff Up	Stuff Up
Setting_B	200K ohm	5.1K ohm

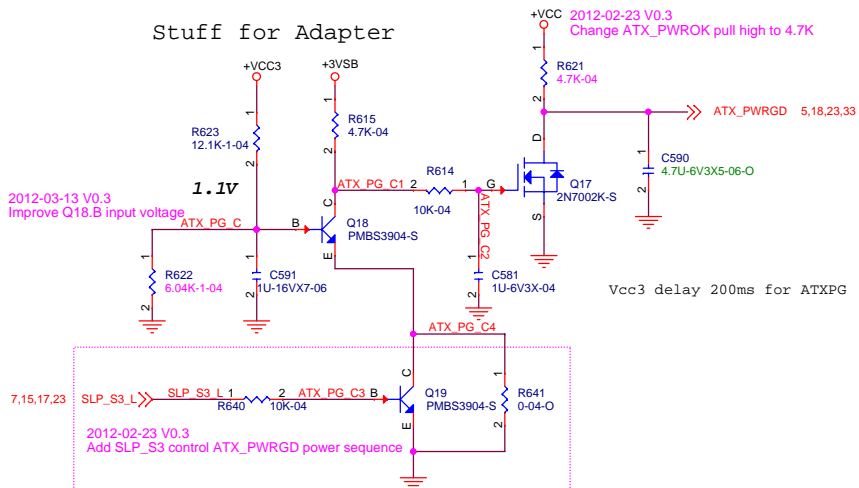


### Dummy Load for ATX power

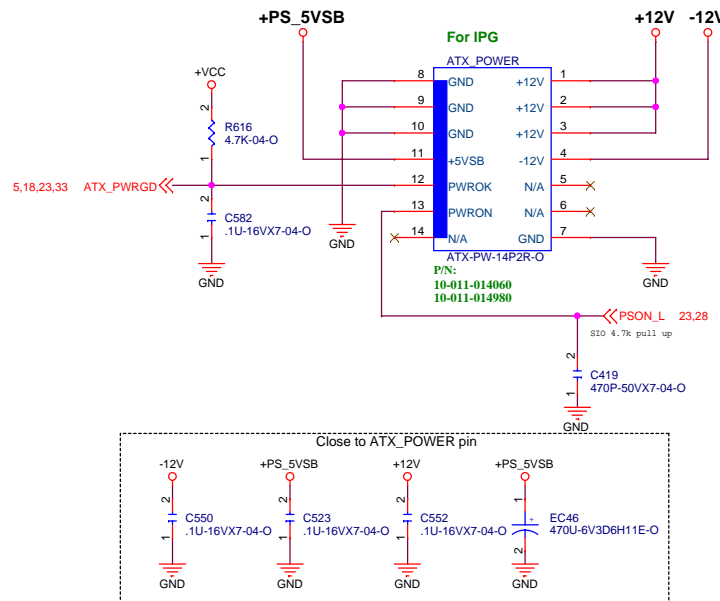


## ATX\_PWRGD

### Stuff for Adapter



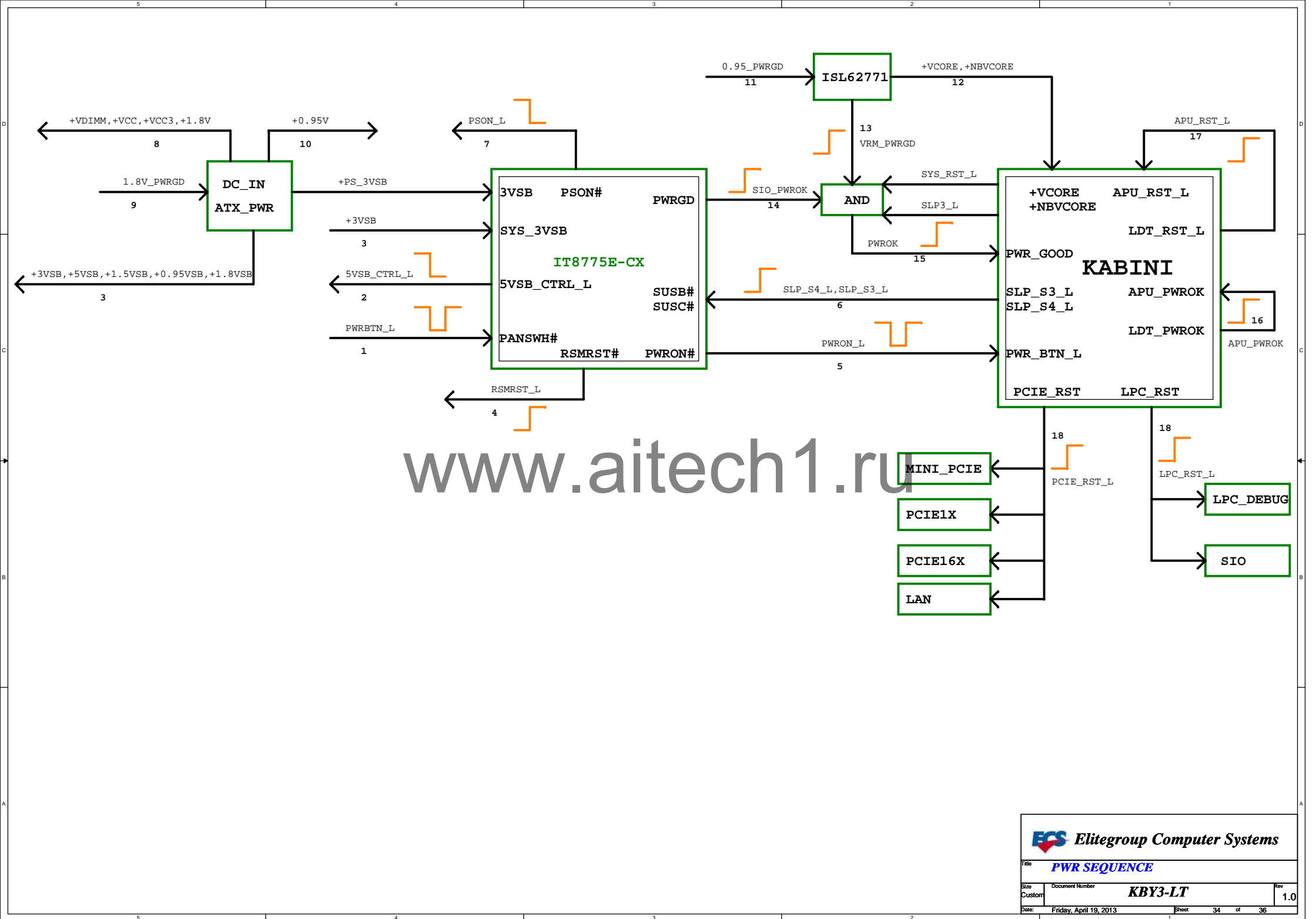
## ATX Power Connector

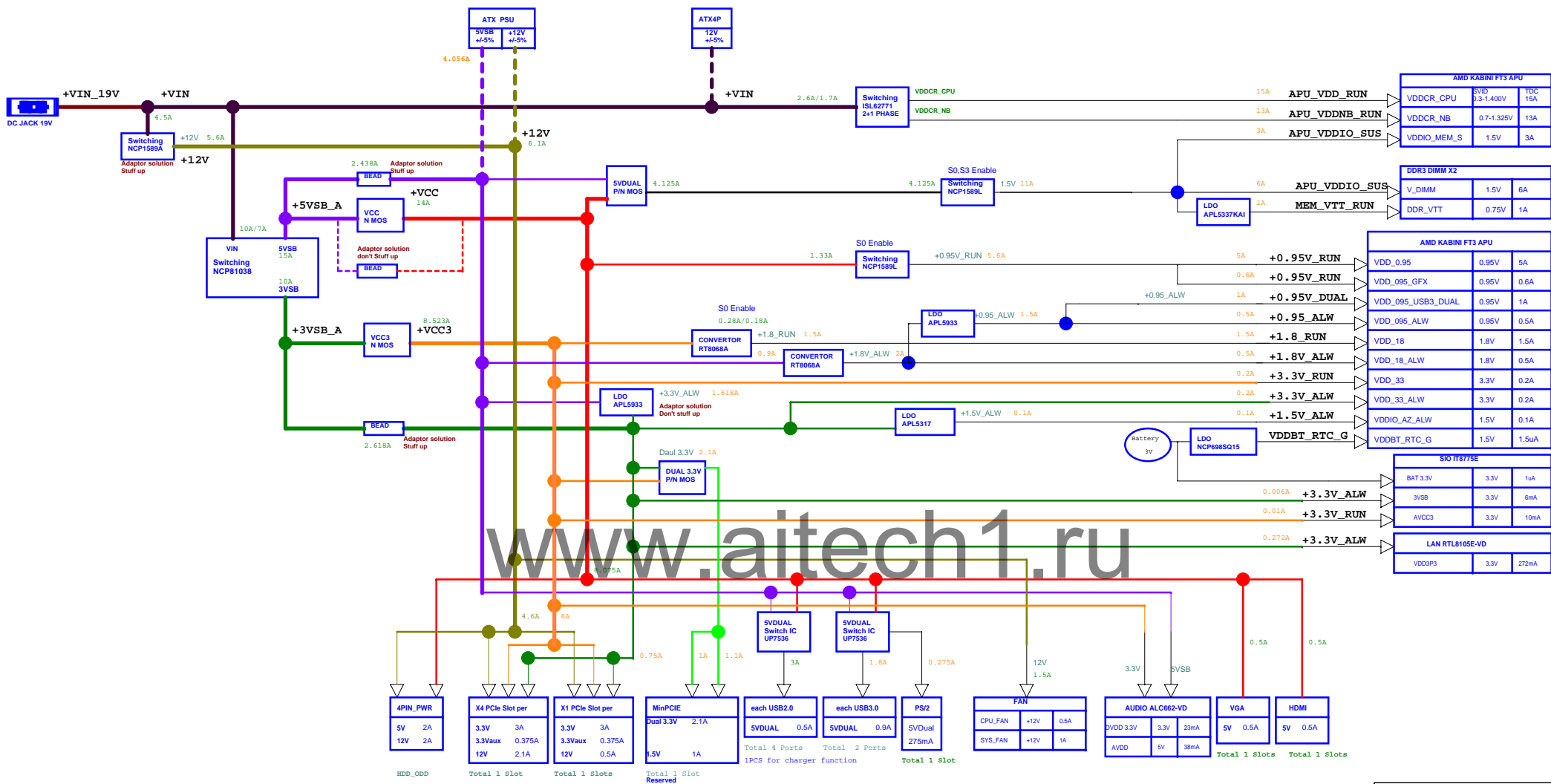


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**DC\_IN\_ATX POWER**

Size Custom Document Number **KBY3-LT** Rev 1.0  
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# REVISION HISTORY:

Rev	Date	Notes	Rev	Date	Notes
A2	11/07/2012	Fisrt released	0.3	02/23/2013	P05.Reserved MINI_PCIE +V1P5_WLAN P05.Reserved RC for PCIE1X SMBUS SI debug P07.Change VGA RGB filter to L-C-L type for SI debug P09.Change R361,R367,R629 to short PAD P11.Add C486,C487 15pF for SMBUS SI debug P11.DIMM1slot is Green,DIMM2 slot is Blue for Lenovo request P16.F_USB3.0 pin A15/A16 power separate follow lenovo request P16.Change C282,C283,C250 footprint P16.Rename F_USB3 to F_USB30 P18.Reserved USBCHA_EN to SIO GP45 P18.Reserved F_USB2 charge function follow MRS P18.Update GPIO168/168/170 control circuit P21.Add F5 for smokeless test P21.Add C94 4.7uF for LAN DC improve P21.Change R343 to 33 ohm for APU_PWROK debug P23.For SI debug,R632=33 ohm,R633=22 ohm P23.Add C611 220pF for PWRON_L glitch P24.Remove SEN_HEADER for Lenovo request P25.Change C466 to 2700pF for VID test issue P26.Remove SC94 for Layout improve P26.Change R368,R313 to 5% component P27.Change R137,R142 to 100K for EUP improve P30.Change U18,U19 footprint to DFN10_PT05_NCP1593 P30.Add EC23 560uF fix LAN surge issue P31.For 1P8V_PWRGD glitch,add C461 0.01uF P32.RTC circuit reserved 0 ohm for Lenovo request P32.Change HDD_ODD_PWR pin4 to GND for Lenovo request P33.DC_IN detect pin connect to GND for Lenovo request P33.Update DC_IN footprint to SMD phase P33.Add SLP_S3 control ATX_PWRGD power sequence P33.Change ATX_PWROK pull high 10K to 4.7K P33.Change R622 to 6.04K improve Q18.B input voltage
0.1	12/11/2012	P05.Change MINI_PCIE V1P5 power solution to LDO APL5933 P06.Add pull high for HDT signal follow AMD SCL V1.05 update P06.Add pull high STEREOSYNC/VGA_HSYNC to fix HDMI no display under OS issue P06.Dumy SVD,SVC,SCT follow AMD SCL V1.05 P06.Add VGA solution for SI fail P07.Change 32.768KHZ capacitance to 18pF for RTC fail P07.Change SYS_PWRGD_R pull high power to +1.8VSB follow AMD SCL V1.05 P08.Add pull high for SPI_CS1 to follow AMD SCL V1.05 P08.Change 48MHZ capacitance to 12pF for crystal test fail P08.Add bypass cap LPCCLK0/LPCCLK1 for EMI P09.+0.95_VDD and +0.95V_GFX bead to 0 ohm P09.Remove some 0402 caps follow AMD SCL P11.Update DIMM SMBUS circuit P11.Change DIMM1 SA0/SA1 setting to follow AMD CRB P13.Add BSS138-S for HDMI_HPD signal to fix leakage to +VCC3 issue P15.Remove +USBPWR_DUAL1 control circuit P15.Change USB_EN2 control signal from +DIMM_DUAL to +VDIMM P16.Add USB_OC control for +USB3_CHA when W/O EZ charge P16.Remove USB3.0 re-driver co-lay 0 ohm P18.Change +USBPWR_DUAL control signal to 3VSBSW_L to fix power drop when S3/S4/S5 to S0 P18.Update USB discharge circuit P19.Remove MONO_OUT circuit component P19.Change R59,R73 to 33 ohm for FSOV fail P21.Change 25MHZ capacitance to 33pF for crystal test fail P23.Add SIO_AVCC3 bleed-off circuit P23.Remove DIMM voltage detect for S3 leakage issue P23.Add RC for SLP3_L/SLP5_L for SI debug P23.Change beep control GPIO to GP31 P23.Reserved RC for LPC bus SI debug P24.Change F_PANEL SATA POWER pull high 165ohm to 330ohm P24.Change SYS_RESET ESD power to connect +3VSB to fix S3 resume fail issue P25.Adjust ISL62771 OCP and compensation P26.Adjust VCORE snubber RC for VDS P26.Change Vcore output cap to 560uF for inrush current issue P27.Change U16 to RT8127GQW P27.Adjust RT8205 OCP and compensation P27.Reserve one cap for RT8127GQW enable P28.Change 12V output EC to 270uF,update footprint to D8 P28.change 12V input and output choke to covered component P28.Add +VCC3 delay circuit follow FT3 power sequence Group C and D P29.Reserve cap for DIMM DUAL circuit P31.Change 0.95V input power to +VCC to increase the Efficiency P32.Update EUP circuit P32.Update RTC power circuit P32.Change RC decrease inrush current P32.Reserved EC for HDD_ODD_PWR +12V and +VCC, change HDD_ODD_PWR connector to black P33.Update DC_IN connector pin define	1.0	04/19/2013	P05.Update +V3P3_WLAN control signal to ATX_PWRGD P06.Update HDT_HEADER footprint to *_NMNP P08.Change C251,C252 to 8.2pF for crystal compatibility P08.Remove SPI ROM socket footprint P06.STEREOSYNC pull high 4.7K to +VCC3 follow function datasheet V1.07 update P12.Update CSJTAG footprint to *_NMNP P13.Improve QN15.G input voltage to 3.9V P15.Reserved R644 +USBPWR_DUAL1 power for USB power control P15.Add RC for +USB2PWR_DUAL1 control P24.Update QN31.B pull high R547 to 2K P27.R168=11.5K for +VCC OCP setting P28.R403=15K for +12V OCP setting P28.Add SLP_S3 contorl +VCC3 power down,QN22 chang e to 2N7002 P29.R596=18.7K for +VDIMM OCP setting P30.Change EC23 to 820uF for LAN surge issue P33.Change DC_IN connector to DIP phase P24.Reserved ESD Cap for SEN_HEADER GPIO

To be update

P07. GPIO49/GPIO51/GEVENT4\_L/GEVENT7\_L need PU/PD 10K follow SCL V1.07



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